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Novel Fault tolerance in Three Stage Solid State Transformer

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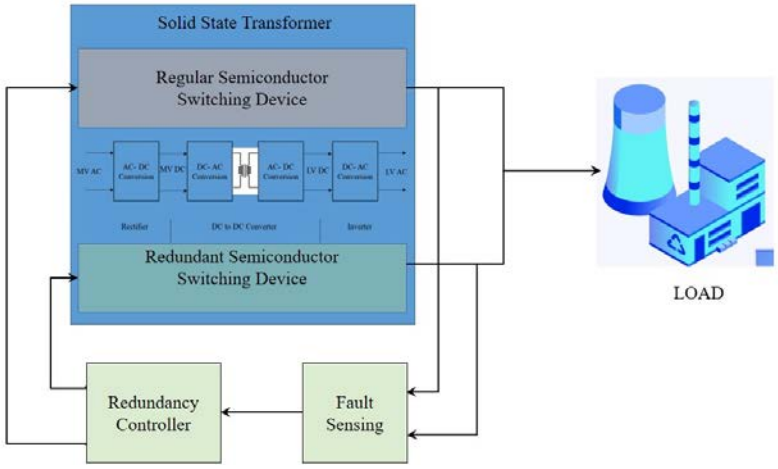
Article

ABSTRACT



Solid State Transformer (SST) have gained a considerable attention of designer and engineers. They offer many advantages over conventional transformer like voltage regulation, compact design, flexibility, high efficiency and power quality. In addition, the SST provides an intermediate DC bus connection between renewable energy sources and storage battery. This enables SST to de deployed in distribution and renewable energy system. In such systems a continuous operation is desired. The power electronics semiconducting switching devices raises a concern about the reliability of SST. A slight over current to the rated capacity of semiconducting devices can damage the SST permanently where a normal transformer's copper winding has capacity to withstand the short circuit current. In this paper, a fault tolerant three stage SST with redundancy is discussed. For fault identification voltage sensing method is deployed for the stages of dual active bridge converter and inverter stages and current sensing method for PWM rectifier stage. Current measurements are done for semiconducting module and voltage measurements are done across the output of each stage. Thresholding is applied to every measured parameter for fault identification. MATLAB simulation is carried out and results are presented.

Keywords: Solid state transformer (SST), fault tolerance, redundancy

INTRODUCTION

In electrical power transmission and distribution transformers are regarded as key functional elements. Transformer is fundamental component of power distribution system. This has naturally attracted researchers to work upon and make it more functional, reliable, efficient and cost effective. Transformers are often subjected to power quality problems like voltage sag and swell, current surges, harmonics and power system faults. To tackle these, many design, optimization and protection techniques have been worked out by designers and engineers.[1] The research on transformer is intended for improving different perspectives, such as efficiency, generalization, and applications. The improvements include incorporating structural prior, designing lightweight architecture, pre-training, and so on.[2] The growing demands of electric vehicle charging, renewable energy and distributed PV generation is further adding to the power quality concerns. For enabling the power grid to take control of these things, a transformer should be sufficiently protected and featured to address these challenges.[3] A solid state transformer (SST) has emerged as a potential solution for conventional transformer.[4] A solid-state transformer (SST) is a power transformer constructed with semiconductor devices instead of the traditional iron core and copper windings. This makes SSTs smaller, lighter, and more efficient than conventional transformers.[5] Despite of being a relatively new technology SST has a great potential to revolutionize renewable and power sector. The fundamentals, topologies, applications and challenges in implementation of SST have been discussed earlier in literature.[6]

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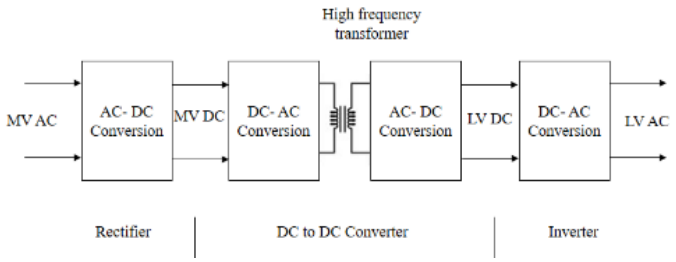

Figure 1. Three stage SST

A SST is built in three stages as shown in figure 1. The first stage is rectifier stage usually constructed with PWM rectifier. The PWM rectifier compensates the harmonics generated in AC – DC conversion with appropriate control scheme.[7] The second stage stands for DC – DC conversion, constructed with dual active bridge (DAB) converter. This stage features to integrate renewable energy systems with grid. The DAB uses medium frequency transformer in the coupling of two active bridges. The third stage stands for DC to AC conversion with inverter. This stage is built for the utilization frequency of 50/ 60 Hz at the level of distribution voltage ranging from 50V to 1000V. The SST can be unidirectional or bidirectional depending upon circuit configuration and control system.

Three state SST topology with modular multilevel converter (MMC) enables the designer to reach higher levels of voltage with lower rated devices. The THD with this topology is reported to be 4.71%.[8] The interfacing of SST in microgrid is subjected to many challenges in terms of converter losses, efficiency, high voltage surge, high-frequency transformer, protection against over voltage and over current, cost and overall control. For control of SST, centralized, decentralized and hierarchical control approaches are practiced depending upon application specific demands.[9] SSTs are specifically designed to operate for locomotive and traction systems, offshore energy generation, smart grid development, integrating DER and ESS, voltage control, reactive power compensation and harmonic mitigation, isolation and fault control, etc.[10]

For a three stage SST the control is also divided into 3 parts i.e. a control scheme each for rectifier, DAB and inverter. The function of rectifier controller is controlling resource current as per reference value without producing harmonics. The function of DAB converter is to regulate the DC link voltage of inverter. The inverter control is often designed to damp oscillations of LC filter and regulate output AC voltage.[11,12] The actual SST deployment requires addressing concerns regarding the grounding designs, protection architecture, maintenance requirements, and cost.[13,14]

The safety and protection of SST is a key issue.[15] The standard protection of SST include surge arresters, breakers and fuses.[16] For designing a sophisticated protection of SST, the over voltage and over current capabilities shall be considered in view of efficiency, power density and cost in order to provide a reasonable protection. The switching devices in SST are often subjected to short circuit and open circuit faults.[17] A serious fault is seen when both the switching devices in same arm of shorted. The open circuit and short circuit fault results in disturbances in the current and voltage waveforms observed across the switching device.[18] The over current and short circuit faults can cause heating of SST components.[19] The SST behaviour under fault[20] provides important insights in fault analysis. The fault analysis algorithm is expected to take feedback of voltage and current at key nodes of SST whereas in case of conventional transformer, the fault analysis is carried out by monitoring leakage inductance and inrush current.[21] The fault ride through control of SST.[22] The fault tolerant control[23] during short circuit fault bypasses the entire faulty module with a healthy to assure uninterrupted operation. Recently, the concept redundancy is being adopted to enhance the reliability of the system. The reliability model[24] of SST is constructed based on topology and different redundancy schemes can be deployed accordingly to address the economy as well. A redundancy design method developed by Li et al.[26] considers reliability and efficiency. The leg replacement strategy[25] for providing redundancy in inverters replaces the entire inverter leg on occurrence of fault. The voltage balancing control[30] based redundancy control bypasses the online power module. The aging of critical power electronics component is reflected in change in thermal data. A thermal model is constructed by Cao et al.[27] for estimating the life time. The modular architecture of SST has 98% operational efficiency.[28,29] The module power balancing strategy[31] maintains same active power in all the modules of a modular SST and prevents over modulation. It is also observed that the most of the SST faults occur in the DC link of SST and researchers have focused on developing fault recognition techniques in DAB[32,33] to take the corrective action.

The redundancy methods studied in the literature provides the redundancy by replacing either entire SST module or a stage or a leg in faulty stage. The techniques are based on current monitoring through the switching devices. In this paper, a device replacement redundancy is proposed which replaces only the faulty switching device in SST with healthy one rather than replacing the entire leg. The proposed system incorporates voltage sensing method in DAB and inverter stage and current sensing method in rectifier stage of the SST. Thresholding techniques are applied for identification of fault. MATLAB simulation results are discussed subsequently to validate the proposed model.

FAULT IDENTIFICATION

Fault Identification with Voltage sensing

The voltage sensing based fault identification is deployed in inverters. The inverter converts DC voltage into AC. Consider a simple three phase inverter as shown in figure 2. Here, Va, Vb and Vc are the three phase voltages measured with respect to neutral.

Let us consider phase voltage Va. The waveforms of phase voltage Va during normal operation of devices Q1 and Q6 is shown in figure 3. Here, it is seen that the voltage waveform is balanced one with equal positive and negative half. Hence the mean value of this waveform can be considered as zero. In case of healthy Q6 and fault in Q1 device, Q1 open circuited and the voltage waveform is observed to appear only in the negative half as shown in figure 4. Here, the mean value of this voltage Va now becomes negative. In case of healthy Q1 and fault in Q6 device, Q6 is open circuited and the voltage waveform is observed to appear only in the positive

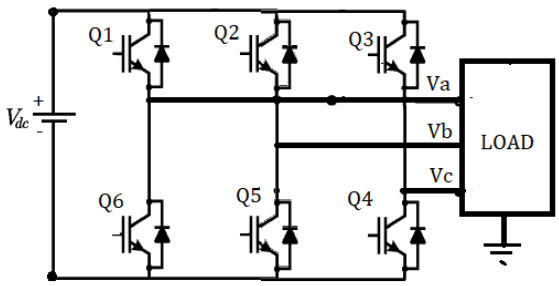

Figure 2. H-bridge inverter configuration

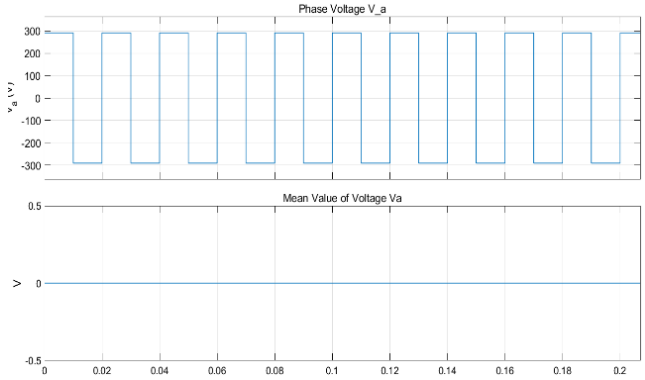

Figure 3. Voltage (Va) waveforms with healthy leg

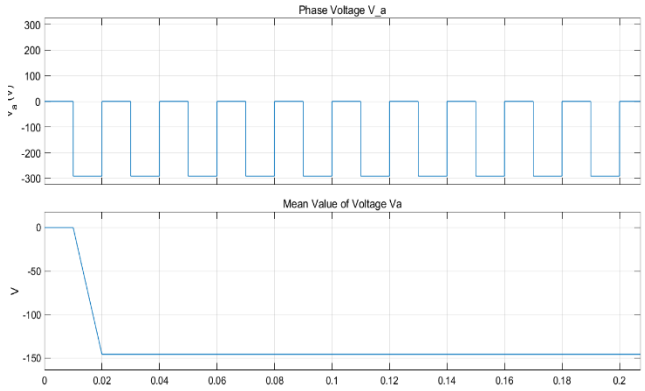

Figure 4. Voltage (Va) waveforms with fault in Q1

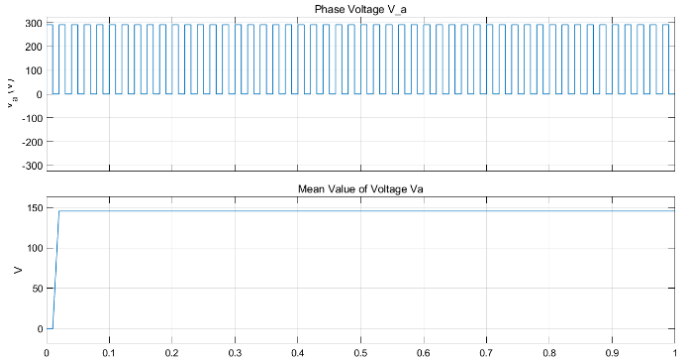

Figure 5. Voltage (Va) waveforms with fault in Q6

half as shown in figure 5. Here the mean value of voltage Va now becomes negative. Thus by measuring the mean value of voltages Va, Vb and Vc, the faults in each of the power electronics switching device can be analysed.

FAULT IDENTIFICATION WITH CURRENT SENSING

For identifying the fault in switching devices with current sensing technique, current measurement is carried out for each of the switching device. In case of healthy device Q1, the instantaneous current is continuous as seen in figure 6. Here, the mean value of current is observed to be positive.

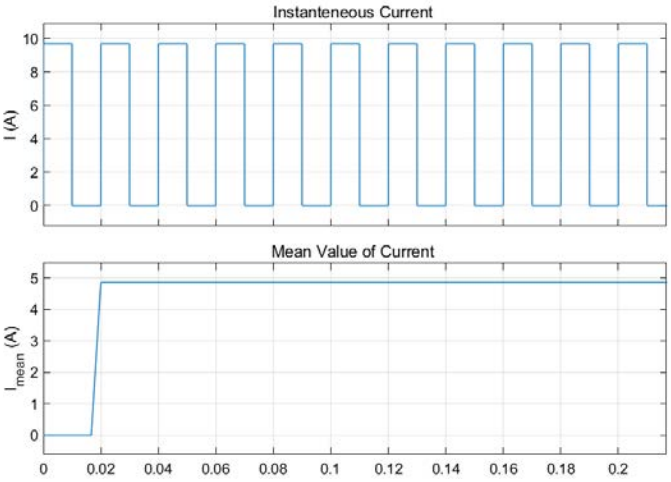

Figure 6. Instantaneous and mean current of healthy Q1

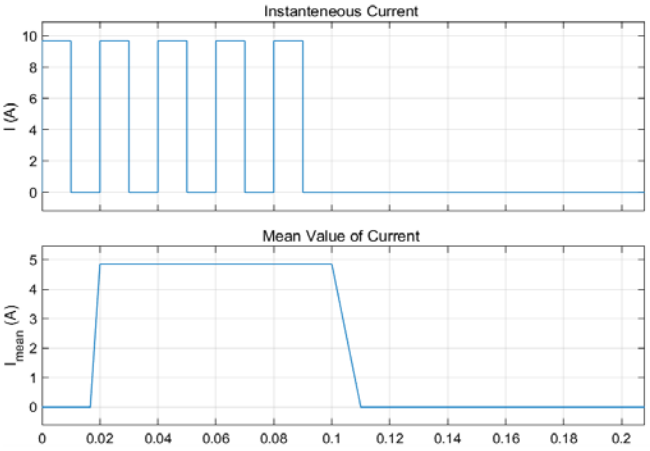

Figure 7. Instantaneous current and mean current in faulty Q1

In case, when open circuit fault occurs in Q1, the current through the device gets blocked and zero current flows through the device as shown in figure 7. Here, an open circuit fault has occurred at t = 0.1 S.

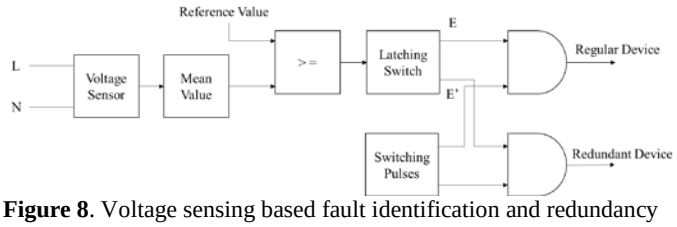

Figure 8. Voltage sensing based fault identification and redundancy control

With the technique of applying thresholds to the measured values of voltage and currents, the fault detection and redundancy control scheme is developed. The figure 8 shows voltage sensing based

fault detection and figure 9 shows current sensing based fault detection.

In voltage sensing based fault identification and redundancy control, voltage sensor measures voltage between line and neutral terminal. The instantaneous value is converted into mean value. This mean value is compared with a predetermined reference value to confirm the occurrence of fault. This fault signal has binary values. It operates a latching switch which provides enable signal to the logical AND gate through which triggering pulses are passed over to either a regular device or redundant device.

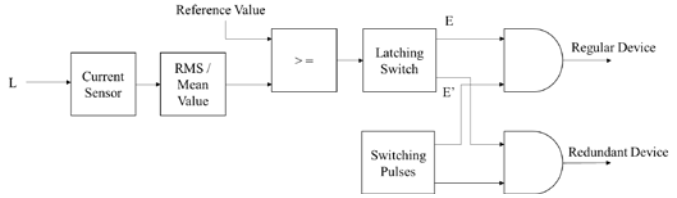

Figure 9. Current sensing-based fault identification and redundancy control

In current sensing based fault identification and redundancy control, a current sensor measures current flowing through each of the switching device. From the instantaneous current, the RMS value is and mean value is computer over one cycle. This RMS and mean value is compared with a predetermined reference value to confirm the occurrence of fault. This fault signal has binary nature. It operates a latching switch which provides enable signal to the logical AND gate through which triggering pulses are passed over to either a regular device or redundant device.

SIMULATION AND RESULTS

The redundancy is deployed for each of the switching device in the power circuit across all the three stages namely PWM rectifier, DAB converter and inverter. A MATLAB model of three stage SST with specification as mentioned in table 1 is developed and simulated for healthy and faulty conditions. The schematics of device level redundancy implementation for power circuit of each stage namely PWM rectifier, DAB converter and inverter is shown in figure 10 (a), 10 (b) and 10 (c) respectively. The simulation model is executed for a period of 1 second. At start all the devices across three stages are healthy. A device fault is created in PWM rectifier at time instance t = 0.3S, in DAB converter stage at t = 0.5S and in inverter stage at t = 0.7S. The waveforms of output voltage of each SST stage are noted as well as the triggering signals of regular and redundant switching devices are also noted.

Table 1. Specifications of three stage SST

PWM Rectifier stage	
Grid Voltage	1100V
Grid Frequency	50Hz
Switching Frequency	10kHz
PWM rectifier output voltage	1200V
Output Capacitor	15mF
Filter (LCL)	L = 500µH, C= 100µF
Fault Detection	Current sensing
Dual Active Bridge Converter stage	
Input Voltage	1200V
Output Voltage	800V
Switching frequency	20kHz
Transformer	880V/880V, 50kVA
DC Link Capacitor	2200 µF
Fault Detection	Voltage sensing
Inverter stage	
Input DC Voltage	800V
3 phase Output Voltage	415V
Switching frequency	2kHz
Output Filter	L = 10mH, C = 500 µF
Fault Detection	Voltage sensing

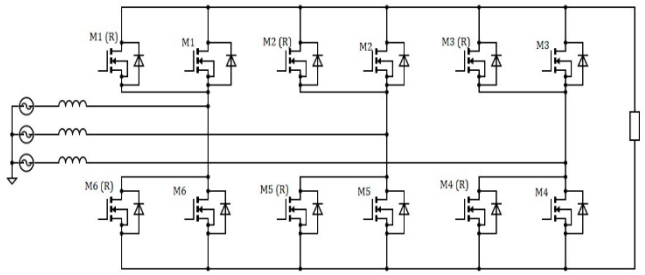

Figure 10 (a) PWM rectifier with device level redundancy

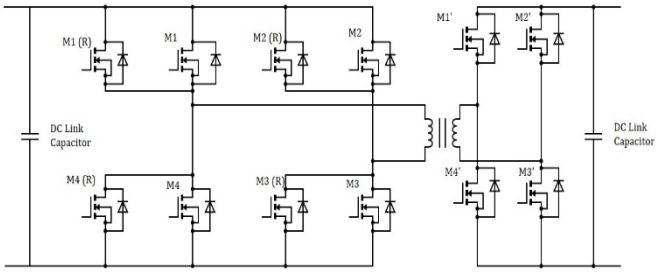

Figure 10 (b) DAB converter with device level redundancy

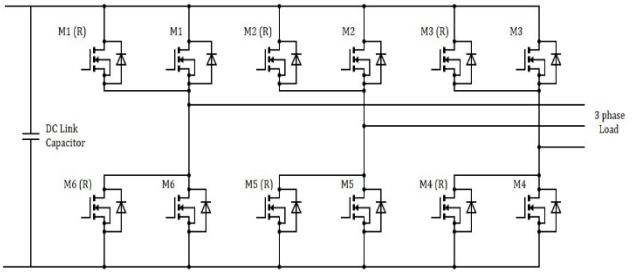

Figure 10 (c) Inverter with device level redundancy

In figure 11 the graph of output voltage of PWM rectifier is shown. Here, a glitch (in the form of swell) is seen at the time instance t = 0.3S. This glitch is due the fault in switching device of the PWM rectifier. The fault recognition system senses the fault with current sensing based fault detection and in response to it, the switching signals are now routed to the redundant device instead of the regular device. This switching of redundant device isolates the faulty device and replaces it with healthy one. Thus the operation of the PWM rectifier and thereby the SST continues

uninterruptedly. The gate triggering pulses of regular and redundant module of PWM rectifier stage are shown in figure 12.

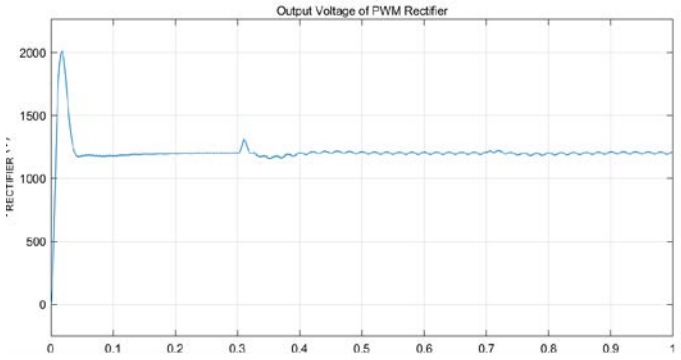

Figure 11. Output Voltage of PWM rectifier

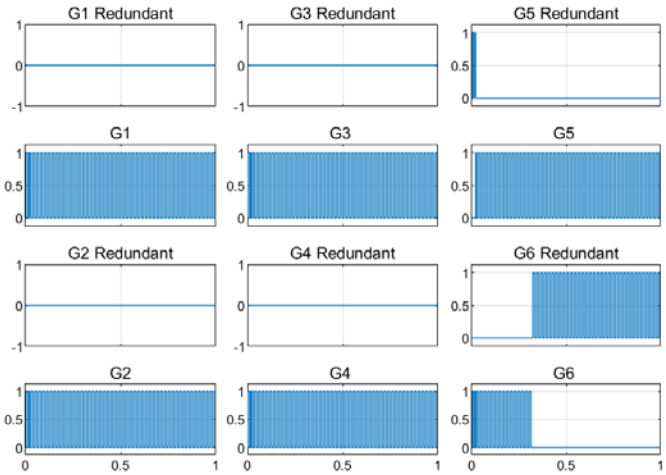

Figure 12. Gate triggering signals of PWM rectifier switching devices

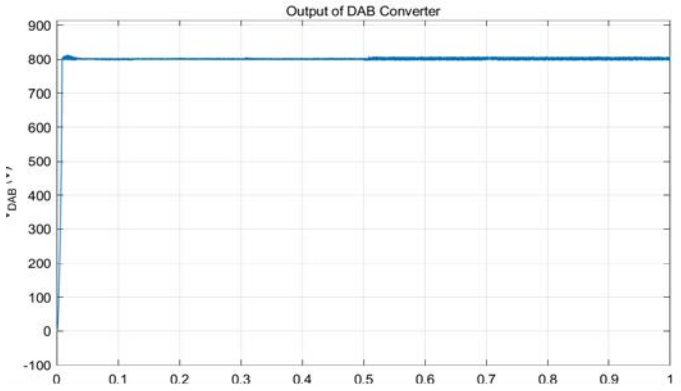

Figure 13. Output voltage of DAB converter stage

At the time instance t = 0.5S, a fault occurring in the DAB stage of SST is reflected in slight deviation in its output voltage as seen in figure 13. This fault is sensed by the voltage sensing based fault recognition and the faulty device is identified by understanding the polarity of the mean value of voltage. Accordingly the triggering pulses are switched from regular semiconductor switching device to the redundancy device.

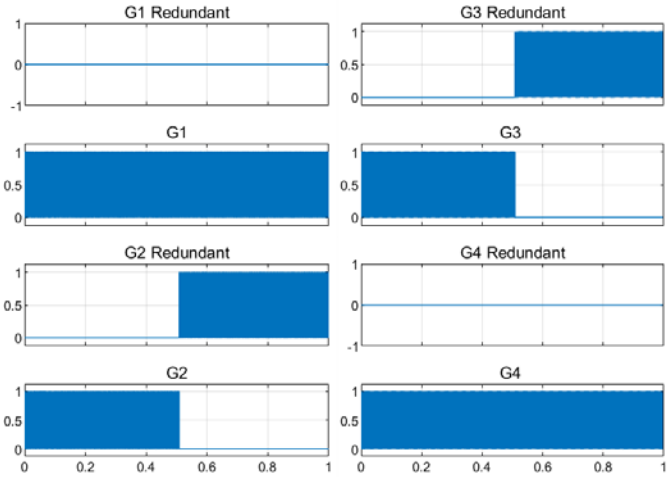

Figure 14. Gate triggering signals of DAB converter switching devices

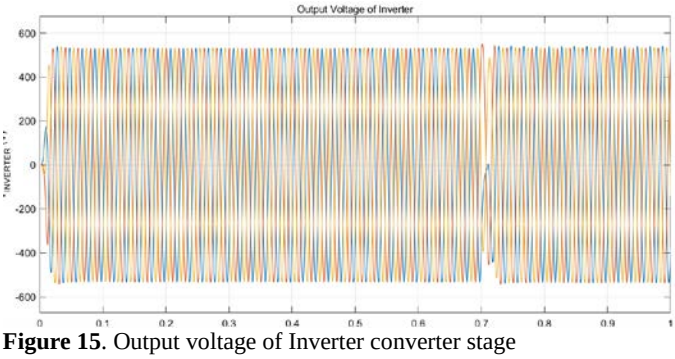

Figure 15. Output voltage of Inverter converter stage

At t=0.7S, a fault is activated in switching devices of inverter stage. The fault in switching device leads to drop in the voltage as seen in figure 15. This fault is identified by voltage sensing based fault recognition and the triggering pulses of faulty switching device are switch to do redundant device. The triggering pulses of regular device and redundant device of inverter are shown in figure 16.

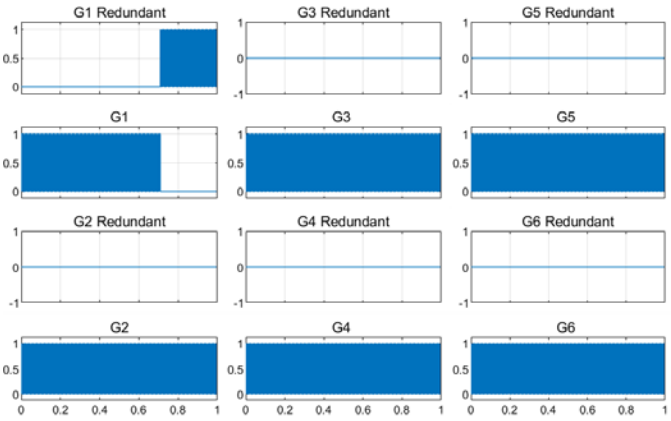

Figure 16. Gate triggering pulses of inverter switching devices

In terms of the output voltage deliverable to the load, It is seen that the distortions due to faults in PWM rectifier stage and DAB converter stage are not reflected in output of SST. The fault in inverter stage only is reflected in output.

CONCLUSION

In modern days the uninterrupted power supply is prime requirement. To ensure uninterrupted operation of SST fault tolerance and redundancy are very much desired features. This paper discusses a novel current and voltage sensing based fault detection technique for a three stage SST for providing redundancy to each power electronic semiconductor switching device in the system. The redundancy feature improves the reliability of overall power system. The fault identification is done by sensing output voltage in DAB and inverter stage and sensing current through each switching device in PWM rectifier stage. Comparison of voltage and current sensor values with threshold reference validates occurrence of fault. The voltage sensing approach is cheaper as compared to current sensing approach. In case of fault the corrective action restores the SST to its normal operation with in single cycle.

CONFLICT OF INTEREST

The authors do not have any conflict of interest.

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