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Error correction and crosstalk avoidance code for Network on Chip Router

Brinda Brahmbhatt, K. M. Dikshitha, P. Abhishek, M. Vinodhini *

Department of Electronics and Communication Engineering, Amrita School of Engineering, Bengaluru, Amrita Vishwa Vidyapeetham, India

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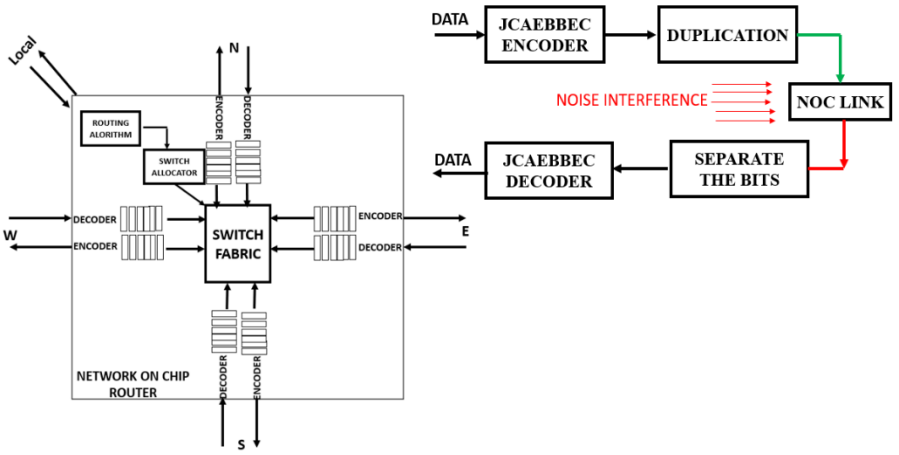
ABSTRACT

In the current multi-core processors, also called System on Chip (SoC), the number of components used in it is increasing in recent days. This indicates a situation that the use of buses is no longer efficient. Now comes the Network on Chip (NoC) with a way to solve this problem. Owing to various noise interference, NoC encounters a huge amount of reliability issues. In nanoscale technology, this issue leads to higher delay and power consumption. To reduce the impact of reliability issues, an error correction coding technique is presented in this paper. Joint Crosstalk Avoidance with Eight Bit Burst Error Correction (JCAEBBEC) is a burst error correction technique followed by duplication in order to avoid crosstalk along with decoding logic that detects and corrects errors. Further, this technique corrects random errors up to 7 bits with approximately 91 % correction capability. Technique corrects burst errors up to 16 bits with 100% correction capability alongside providing crosstalk avoidance. Furthermore, the implementation results show that the JCAEBBEC technique attains lesser area, power and delay compared with the existing techniques.



Keywords: Coding Techniques, Communication Links, Error Control, Hamming code, Network on Chip, Parity bits, System on Chip

INTRODUCTION

Network-on-Chip (NoC) is a structured communication arrangement that is used to interlink several units in a System-on-Chip (SoC). A standard NoC architecture mainly involves Intellectual Property (IP), Router and a Network Interface (NI) or Network Adapters (NA).[1-4] The IP does the job of processing the data it receives. This is also sometimes referred to as a 'core' in multicore processor architecture.

The NoC connects multiple components present on a chip and facilitates data transfer from one component to another in the form of packets.[5-8] The various components of NoC interconnect links, routers and NIs.[9-13] The router intern has many components involved, namely the routing module, arbitration module and crossbar switch. A routing algorithm is used by the router to make the routing decision for the packets. The NI connects the router and IP module and does the job of converting the data from IP to a form that the router can interpret.

All the components contribute to the communication in NoC as follows; Links connect the router physically while the router communicates the data following a suitable protocol. The NA separates the communication activities from the computation activities.[14] The reliability of the system depends on how efficiently these interconnect links function. NoC fetches the benefit of modularity, structural consistency, scalability and effectual communication. However, owing to elevated clock frequencies, scaling of supply voltage, shrinking size, faster clock rates and manufacturing defects they encounter a huge amount of reliability issues. Therefore, in nanoscale technology, this issue leads to higher delay and power consumption.[13,15,16] To reduce the impact of reliability issues error correction coding techniques are normally proposed. Reliability issues increase with deep sub-micron

*Corresponding Author: Dr. M. Vinodhini
Email: m_vinodhini@blr.amrita.edu

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technology noises. Generally, crosstalk avoidance is merged with the error correction technique to increase the error correction capability.[17-18]

In order to reduce the crosstalk effects and random and burst errors as well either link bandwidth or link power consumption is increased. The proposed method overcomes this issue by outperforming in all three aspects like area, power and delay. The proposed method Joint Crosstalk Avoidance with Eight Bit Burst Error Correction (JCAEBBEC) is a burst error correction technique followed by duplication in order to avoid crosstalk along with decoding logic that detects and corrects 16-bit burst errors, 8 bits in each copy, with 100% correction capability. It also corrects 7-bit random errors considering both the copies together with approximately 91 % correction capability.

Related Works

A number of coding techniques have been introduced so as to account for error correction and crosstalk avoidance.[19-22] Consequently, Crosstalk Aware Transient Error Correction (CATEC) coding technique manages the reliability issues and also reduces the switching activities which are flit-dependent. It corrects up to 2 error bits and a few patterns up to 9 error bits. Further, algorithms for self-calibration and rerouting are also included with the technique to attain higher power efficiency.[14] This inclusion helps in correcting single-bit random and burst errors up to five bits as well. This technique handles crosstalk by doing triplication. A parity coding technique, Multi-bit Error Correction coding with Crosstalk avoidance using the Parity Sharing technique (MECCPS) corrects burst or random errors up to 24 bits.[23]

Joint Crosstalk Avoidance with Multiple Bit Error Correction (JCAMEC) techniques improves error correction and avoids crosstalk as well.[17] JCAMEC applies duplication over the data which are encoded using extended Hamming and parity check codes. This procedure helps in the process of avoiding crosstalk and is suitable to tackle burst errors. Joint crosstalk-aware Multiple Error Correction (JMEC) coding techniques focus on the reduction of burst errors.[15] A simple coding scheme concurrently focuses on crosstalk effects and also detects up to 7 random errors by the inclusion of duplication.[24] Another coding technique that reduces crosstalk is proposed.[18] This technique uses triplication to tackle crosstalk and uses a parity check to enhance the correction probability. Multibit Random and Burst Error Correction (MBRBEC) technique manages multi-bit random and burst errors.[25] This technique corrects any patterns up to 5 bits and also uses triplication to avoid crosstalk. Energy efficient error correction techniques like reducing operating voltage are proposed.[14,26-27] Co-management method that controls both transient and permanent errors without additional wires is proposed.[28] An adaptive error control coding technique is proposed. [29]

In all the coding techniques that are surveyed, either one of area, power and delay is compromised while increasing the reliability of the NoC links. Crosstalk Aware Transient Error Correction (CATEC) code can only correct 1 or 2 error bits and a few error patterns up to 6 to 9 error bits.[9] In Self Calibrated Power Efficient Five-bit Burst Error Correction (SCPEFBEC), to increase the correction probability and to reduce the crosstalk, link bandwidth is increased.[14] However, a slight decrease in area, power and delay is attained even though the errors corrected are more in MECCPS. Duplicated Two-Dimensional Parities (DTPD) can detect up to 7 errors as it uses an automatic repeat request methodology. MECCPS approach is having slight area overhead when compared to DTPD. In JCAMEC, a new approach is used to correct and detect errors in hop-to-hop but it can correct up to only 4 bits. JMEC can correct up to 10 random errors. However, the technique is not suitable for managing burst errors. In report by M. Maheswari et.al.,[25] the approach can only correct 1 and 2-bit errors and 3-bit errors to some extent. MBRBEC can correct only up to 5-bit errors.

In the proposed JCAEBBEC method, to be more power efficient and to reduce the overhead, data bits are arranged in rows and columns and Hamming method is used to encode. In order to avoid crosstalk, duplication is performed. The results attained prove that the technique corrects burst errors of 16 bits (both copies included) with 100% correction capability, random errors of 3 bits with 100% correction capability and up to 7 random errors with 90.64 % correction capability. Performance analysis of JCAEBBEC is compared with other states of work including CAEDEC, JMEC and DTDP-7ED.

Current work

The novel coding technique is proposed in JCAEBBEC. The proposed work is a burst error correction technique followed by duplication in order to avoid crosstalk along with decoding logic detects and corrects 16-bit burst errors, 8 bits in each copy, with 100 % correction capability. It also corrects 7-bit random errors considering both the copies together with approximately 91 % correction capability.

JCAEBBEC ENCODER

The JCAEBBEC encoder is a multi-bit burst and random error correction technique that uses Hamming code to encode the given data bits. These bits are arranged in rows and columns called the Hamming matrix and the row-wise Hamming technique is performed. Redundant bits in each row are calculated.[30] This results in 24 redundant bits for overall 32 bits. The encoded bits are sent to the duplication block which is used to avoid crosstalk as shown in Figure 1.

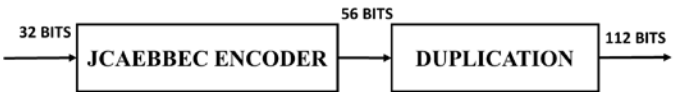

Figure 1. JCAEBBEC Encoder

JCAEBBEC ENCODING PROCESS

The JCAEBBEC encoder uses Hamming code to correct multi-bit bursts and random errors. The fundamental principle of the Hamming code allows identifying of a single error by the inclusion of extra parity bits. The 32 data bits are arranged column-wise as shown in Figure 2. This is called the Hamming matrix and performs row-wise Hamming. Each row has 4 data bits, so Hamming code generates 3 redundant bits for each row by performing XOR on the data bits. As there are 8 rows in total it results in 24 redundant bits.

M0	M8	M16	M24
M1	M9	M17	M25
M2	M10	M18	M26
M3	M11	M19	M27
M4	M12	M20	M28
M5	M13	M21	M29
M6	M14	M22	M30
M7	M15	M23	M31

Figure 2. Hamming matrix

The redundant bits are calculated as follows.

For 1st row,

R0=M0 XOR M8 XOR M24 (1)

R1=M0 XOR M16 XOR M24 (2)

R2=M8 XOR M16 XOR M24 (3)

For 2nd row,

R3=M1 XOR M9 XOR M25 (4)

R4=M1 XOR M17 XOR M25 (5)

R5=M9 XOR M17 XOR M25 (6)

and so on.

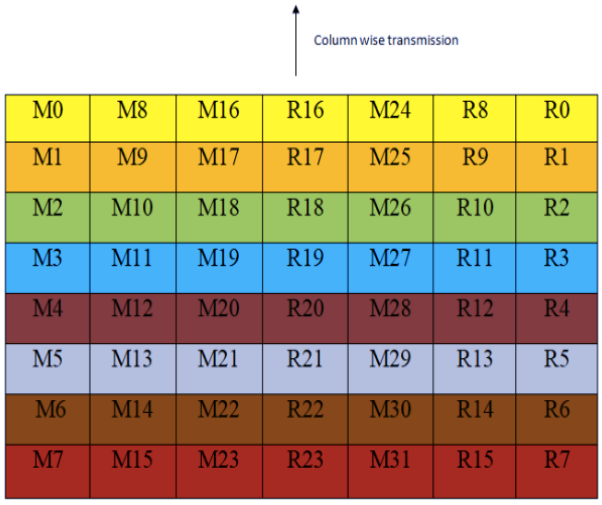

Figure 3. Transmission of message bits

A total of 56 bits are sent to a duplication unit in order to avoid the crosstalk. The two sets of 56 bits are sent column-wise during transmission as shown in Figure 3. The message and redundant bits are arranged as follows in the 56 bits.

Duplication

The encoded bits from the JCAEBBEC encoder are 56 bits. This is duplicated to reduce crosstalk. In the end, all 112 bits which comprise 2 copies of 56 encoded bits and 2 sets of parity bits are communicated. The data0 of copy I encoded bits runs adjacent to the data0 of copy II encoded bits and so on. The method of duplication of encoded bits and sending the same copies of bits through adjacent channels minimizes the crosstalk effects very effectively.[14]

JCAEBBEC DECODER

The JCAEBBEC decoder is used to correct both burst and random multi-bit errors. The JCAEBBEC decoder comprises one group separator, two JCAEBBEC decoders and the multiplexer at the end. The group separator separates the 112 encoded bits into two 56 data bits as shown in Figure 4.

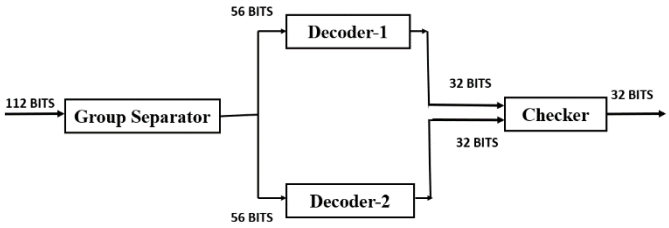

Figure 4. JCAEBBEC Decoder

JCAEBBEC DECODING PROCESS

A total of 112 bits is received at the decoder. JCAEBBEC decoder first computes the syndrome values by XOR-ing the message bits with the redundant bits in each row. The calculation of syndrome values is done as follows.

For 1st row,

S0=R0 XOR M0 XOR M8 XOR M24 (7)

S1=R1 XOR M0 XOR M16 XOR M24 (8)

S2=R2 XOR M8 XOR M16 XOR M24 (9)

For 2nd row,

S3=R3 XOR M1 XOR M9 XOR M25 (10)

S4=R4 XOR M1 XOR M17 XOR M25 (11)

S5=R5 XOR M9 XOR M17 XOR M25 (12)

and so on.

Error-free data bits are received if the syndrome bits are all zero. Else it gives the location of the bit that is corrupted. The bits in the copy that are corrupted are corrected and sent to the checker as shown in Figure 4 which chooses the copy to be selected based on the number of errors.

This gives four different scenarios as follows:

- When there is no error in the copy, the checker can select any of the copies either copy I or copy II.
- When there are errors within the range of correctability in both copies, the checker can choose any copy, either copy I or copy II.
- When there are errors within the range of correctability in one of the copies, the checker will choose that copy.
- When there are errors out of range in both copies, the checker will not select any copy as errors are out of range.

The possible combinations of random and burst errors that the decoder can decode along with the percentage of correction are given in Table 1. It is seen from Table 1 that the percentage of error correction for burst errors of 16 bits is 100%. In the first copy, burst errors are correctable up to 8 bits. Hence, any number of burst errors lesser than 8 bits in one copy is 100% correctable. Based on this logic, it is said that if the second copy has burst errors lesser than or equal to 8 bits, it is 100% correctable.

Table 1. Random and burst errors correction capability of the JCAEBBEC technique

Total number of burst errors in both the copies	Number of errors in the first copy	Number of errors in the second copy	Correction capability
Max. 16-bit burst	1,2,3,4,5,6,7,8 bit burst	1,2,3,4,5,6,7,8 bit burst	100%
Max. 16-bit burst	1,2,3,4,5,6,7,8 bit burst	Any bits of random error	100%
Max. 16-bit burst	Any bits of random error	1,2,3,4,5,6,7,8 bit burst	100%

Table 2. Two and three-bit random errors correction capability of the JCAEBBEC technique

Two-bit random errors		Three-bit random errors		Correction Capability
Copy I	Copy II	Copy I	Copy II	
0	2	0	3	100%
2	0	3	0	
1	1	1	2	
-	-	2	1	

Further, if the second copy has random errors (any number of random errors), it is 100% correctable.

The error correction for random errors is calculated and shown in Tables 2, 3, 4, 5 and 6. In Table 2, correction capability for two and three-bit random errors are illustrated with possible combinations of errors occurring in both copies. The JCAEBBEC technique has 100% correction capability for 1-bit, 2-bit and 3-bit random errors. From Table 2, it is seen that if a 2-bit random error occurs anywhere in copy II, then it is 100% correctable. Similarly, if a 3-bit random error occurs solely in copy II, it is 100% correctable. In Table 3, the error correction capability for four-bit random errors is given with its possible combinations of occurrence in both copies. The probability of occurrence for each combination is given along with the average error correction capability for all the four-bit random errors. It is seen in Table 3 that if a 4-bit random error occurs anywhere in copy II, then it is 100% correctable. If a 2-bit random error occurs in copy I and a 2-bit random error occur in copy II, then it is 90.32% correctable. All the error correction capabilities are averaged to get an average error correction capability of 98.064% for four-bit random errors. In Table 4, error correction for five-bit random errors is given. Its possible combinations of occurrence in both copies are listed. The probability of occurrence for each combination is given along with the average correction capability for five-bit random errors.

Table 3. Four-bit random errors correction capability of the JCAEBBEC technique

Four-bit random error		Correction capability	Average correction capability
Copy I	Copy II		
0	4	100%	
4	0	100%	
1	3	100%	98.064%
3	1	100%	
2	2	90.32%	

Table 4. Five-bit random errors correction capability of the JCAEBBEC technique

Five-bit random error		Correction capability	Average correction capability
Copy I	Copy II		
0	5	100%	
5	0	100%	
1	4	100%	96.77%
4	1	100%	
2	3	90.32%	
3	2	90.32%	

Table 5. Six-bit random errors correction capability of the JCAEBBEC technique

Six-bit random error		Correction capability	Average correction capability
Copy I	Copy II		
0	6	100%	
6	0	100%	
1	5	100%	
5	1	100%	93.27%
2	4	90.32%	
4	2	90.32%	
3	3	72.25%	

It is seen in Table 4 that if a 5-bit random error occurs anywhere in copy II, then it is 100% correctable. Similarly, if a 2-bit random error occurs in copy I and a 3-bit random error occur in copy II, then it is 90.32% correctable. All the probabilities are averaged to get an average correction capability of approximately 97% for all combinations of five-bit random errors.

In Table 5, error correction for six-bit random errors is given. The probability of occurrence for each combination is given along with the average correction capability for all the six-bit random errors. It is seen in Table 5 that if a 6-bit random error occurs anywhere in copy II, then it is 100% correctable. If a 2-bit random error occurs in copy I and a 4-bit random error occur in copy II, then it is 90.32% correctable. If a 3-bit random error occurs in copy I and a 3-bit random error occur in copy II at the same time, then it is 72.25% correctable. All the probabilities are averaged to get an average correction capability of 93.27% for all various combinations of six-bit random errors.

Table 6. Seven-bit random errors correction capability of the JCAEBBEC technique

Seven-bit random error		Correction capability	Average correction capability
Copy I	Copy II		
0	7	100%	
7	0	100%	
1	6	100%	
6	1	100%	90.64%
2	5	90.32%	
5	2	90.32%	
3	4	72.25%	
4	3	72.25%	

In Table 6, error correction for seven-bit random errors is given along with the possible distributions of seven-bit random errors in both copies. It is seen in Table 6 that if a 7-bit random error occurs anywhere in copy II, then it is 100% correctable. If a 2-bit random error occurs in copy I and a 5-bit random error occur in copy II, then it is 90.32% correctable. If a 3-bit random error occurs in copy I and a 4-bit random error occur in copy II at the same time, then it is 72.25% correctable. All the probabilities are averaged to get an approximate probability of 91% for all various combinations of seven-bit random errors.

Performance Analysis and Evaluation

All the simulations were performed using the Modelsim tool and the designs were verified for the logic. The total dynamic power, critical path delay and the total area occupation of the techniques have been calculated by using the Cadence genus design compiler tool and mapped onto a 45 nm technology library for '32' bit data. Furthermore, the assessment of the parameters has been done for the encoder and decoder together with a relative comparative study to examine them. The appropriate analysis illustrates our findings for each parameter and is discussed in this section.

Reliability Evaluation

The noise that affects the on-chip interconnect can be analyzed by using the conventional error model, which is an additive white noise Gaussian function. The Bit Error Probability (BEP) (ϵ) of a wire is given by the relation:[10]

$$\epsilon = Q\left[\frac{V_{dd}}{2\sigma_n}\right] \tag{13}$$

The Q-function is

$$Q = \int_{\frac{V_{dd}}{2\sigma_n}}^{\infty} \frac{1}{\sqrt{\pi}} e^{\frac{-y^2}{2}} dy \tag{14}$$

Link supply voltage and noise standard deviation are taken as V_{dd} and σ_n respectively. For the calculation of the bit error rate in the above-mentioned model, the link supply voltage is assumed as 1.1 V and σ_n ranges from 0.04 and 0.2. Further, the single wire error probability is assumed to be statistically independent. In off-chip networks, received data quality is estimated and analyzed with the help of the residual error probability. As per the survey, the same way of analysis is carried over in on-chip interconnects as well. The complement of the probability of decoding the data at the destination without errors $P_{correct}$ gives the probability of residual flit error rate $P_{residual}$. This is given by[10]

$$P_{residual} = 1 - P_{correct} \tag{15}$$

In the high noise environment, the residual flit error rate probability considering only random errors for the small value of is obtained by[10]

$$P_{residual} = \binom{2N}{8} \epsilon^2 \tag{16}$$

Figure 5 illustrates the residual error probability as a function of σ_n for various techniques. It is observed in Figure 5 that the curve for the JCAEBBEC technique is the least compared to other techniques. Consider a noise standard deviation of 0.14. The probability value of our proposed work is $5.2\text{x}10^{-24}$, whereas that of CAEDEC is $1.15\text{x}10^{-11}$, JMEC is $1.53\text{x}10^{-11}$ and DTDP is $8.52\text{x}10^{-12}$. It is seen that the probability value of our work is the lowest compared to all the other techniques.

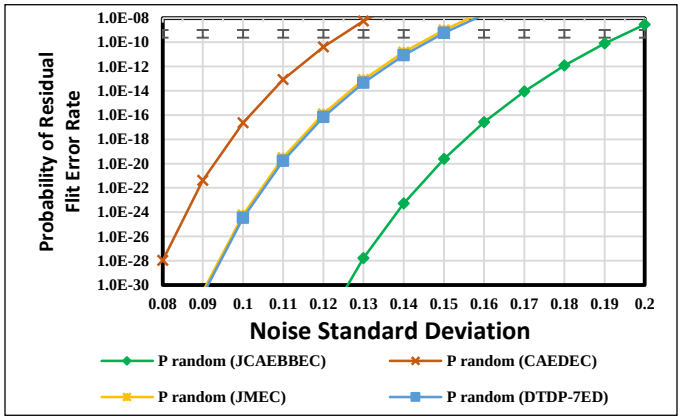

Figure 5. Probability of residual error rate versus noise standard deviation

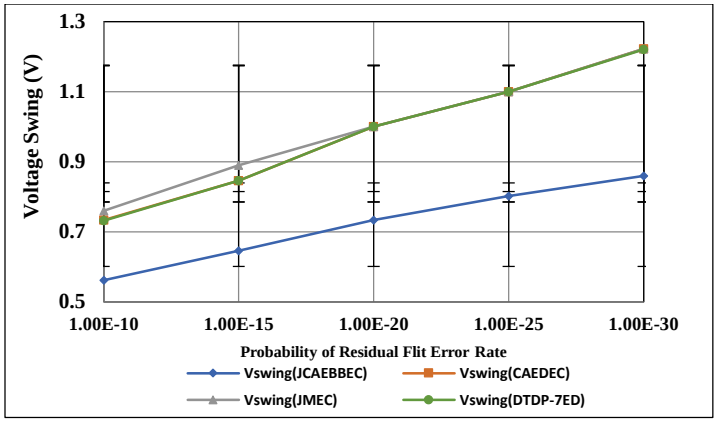

Figure 6. Voltage swing reduction versus residual flit error rate probability

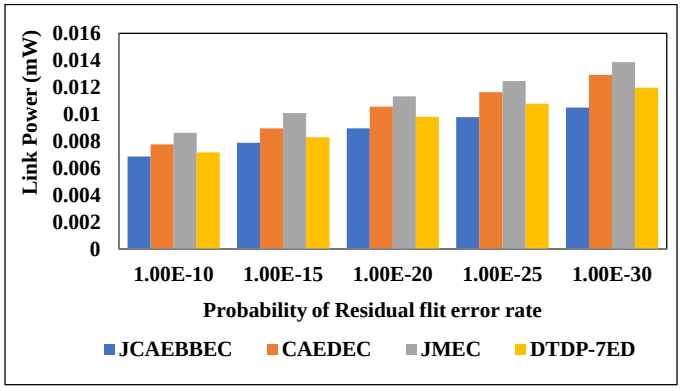

Figure 7. Link power consumption versus probabilities of residual flit error rates

Link Swing Voltage

Link swing voltage is calculated using the equation given below [10]

$$V_{swing} = 2\sigma_n Q^{-1}(\epsilon) \tag{17}$$

The inverse Q function $P_{residual}$ value at which the below-given equation is satisfied is taken in the analysis.[10]

$$P_{residual}(\epsilon) = P_{req}, \quad (18)$$

P_{req} is the expected flit error rate. The link swing voltage of the JCAEBBEC technique is compared with the CAEDEC, JMEC and DTDP-7ED techniques as shown in Figure 6. It illustrates the reduction in voltage swing as a function of residual flit error rates. In Figure 6, it is seen that the curve for the JCAEBBEC is the lowest compared to the other techniques. Since the voltage swing values of certain techniques are the same for some probabilities, it is observed that the curves overlap with each other. In Figure 6, it is noticed that the values of CAEDEC and JMEC are almost similar. Hence, the curves superimpose one another in Figure 6. For a probability of $1.0x10^{-10}$, JCAEBBEC has a voltage swing of 0.562V, CAEDEC has a V_{Swing} of 0.734V, JMEC has 0.76V and DTDP-7ED has 0.732V. JCAEBBEC technique has the least value of voltage swing than other techniques.

Link Power Consumption

The link power consumption is calculated as [10,25]

$$P_L = \alpha C_L W_L V_L f_{clk} \quad (19)$$

The switching activity α is taken as 0.5 in the calculations. The link capacitance and the width of the data are taken as C_L and W_L respectively. f_{clk} is the clock frequency. In the JCAEBBEC technique, link capacitance and clock frequency are considered 218 fF and 1 GHz respectively. The link power consumption of the JCAEBBEC technique is compared with CAEDEC, JMEC and DTDP-7ED techniques as shown in Figure 7. It is noticed in Figure 7 that the value of link power consumption for the JCAEBBEC technique is consistently lower compared to the other techniques. For a probability of

$1.00x10^{-10}$, it is observed that the link power consumption for JCAEBBEC, CAEDEC, JMEC and DTDP-7ED is 0.0068mW, 0.0077mW, 0.0086mW and 0.0071mW respectively. The link power consumption of the proposed method is the lowest.

Table 7. Error correction capability of burst and random errors

No. of errors	JCAEBBEC	CAEDEC	JMEC
Burst errors up to 16(both copies)	100%	0%(only up to 3 bits 100%)	0%(only up to 3 bits 100%)
Random errors up to 2 bits	100%	100%	-
Random errors up to 3 bits	100%	70%	-
Random errors up to 4 bits	98.06%	-	-
Random errors up to 5 bits	90.77%	-	-
Random errors up to 6 bits	93.27%	-	-
Random errors up to 7 bits	90.64%	-	-

Error Correction Capability

The error correction capability is compared with CAEDEC, JMEC and DTDP-7ED as shown in Table 7. Since DTDP-7ED is an ARQ technique and it only detects errors, not corrects them, it is not included in Table 7. It has 0% error correction capability as it doesn't support error correction. From Table 7 it can be seen that not only does JCAEBBEC provide a high level of burst error correction, but its intelligent arrangement of data in the matrix allows it to also provides a high level of correction probability for a higher number of random error which other coding schemes do not provide.

Cost Function Analysis

Generally, the cost function is estimated based on the Power Delay Area Product (PDAP), Energy Delay Area Product (EDAP) and Power Delay Product (PDP).[11] Further, the cost function on the implementation parameters of the technique. Overall, all these are considered the most important figure of merit for the analysis of the performance of the technique.

PDP is the product of power dissipation (P_d) and combinational path delay (t_p) and is given as[14]

$$PDP = P_d t_p \quad (20)$$

Using the formula in equation 8 the Power Delay Product (PDP) in mW.ns is calculated as shown in Table 8. It is observed from Table 8 that the PDP value of JCAEBBEC and CAEDEC is the lowest among all the techniques. The higher value of PDP for the JCAEBBEC technique is compensated by its high error correction capability whereas CAEDEC is able to correct and detect only 3-bit errors. PDAP is a metric that is used to estimate the cost function of the JCAEBBEC technique. This is the product of power dissipation (P_d), combinational path delay (t_p) and Area (A) which is expressed as [11]

$$PDAP = P_d t_p A \quad (21)$$

Using the formula in equation 9, Power Delay Area Product (PDAP) in $mW.ns.\mu m^2$ is calculated as shown in Table 9. From Table 9, it is observed that the proposed coding technique has a lower value of PDAP. Whereas, when compared with the CAEDEC technique, the higher value of the JCAEBBEC technique is compensated by it's higher ability to detect and correct more errors.

Table 8. Power Delay Product Comparison of different techniques

Techniques	PDP (nW.ps)
JCAEBBEC	0.0308
CAEDEC	0.0096
JMEC	0.0518
DTDP-7ED	0.0420

Table 9. Power Delay Area Product Comparison of different techniques

Techniques	PDP ($mW.ns.\mu m^2$)
JCAEBBEC	118.9496
CAEDEC	42.9498
JMEC	337.9834
DTDP-7ED	183.1336

Table 10. Energy Delay Area Product Comparison of different techniques

Techniques	PDP ($mW.ns^2.\ \mu m^2$)
JCAEBBEC	47.5798
CAEDEC	29.6344
JMEC	239.9682
DTDP-7ED	111.7115

A combination of metrics like performance and PDAP results in the analysis of cost performance. The EDAP is the product of PDAP and combinational path delay (t_p) which is expressed as

$$EDAP = (PDAP)t_p \quad (22)$$

Using the formula given in equation 10, Energy Delay Area Product (EDAP) in $mW.ns^2.\mu m^2$ is calculated as shown in Table 10. It is noticed that the value of the proposed work is way lesser compared to JMEC and DTDP-7ED. The difference in the values is almost 10^2. Compared with the CAEDEC technique, it is seen that the EDAP value is higher, which is compensated by the higher reliability of the technique as discussed in the previous sections.

CONCLUSION AND FUTURE WORK

The system on the chip is subjected to different sources of errors. This impact is greatly increasing in recent technologies. By placing the error control technique inside the router and by communicating the same set of bits through parallel wires, both the reliability and crosstalk issues are tackled. The results of the JCAEBBEC technique are evaluated and performance is discussed and compared. JCAEBBEC technique has low swing voltage and link power consumption compared with other techniques. Further, the implementation results show that the JCAEBBEC technique attains lesser area, power and delay compared with the CAEDEC, JMEC and DTDP-7ED techniques. JCAEBBEC technique corrects burst error of 16 bits from both copies with 100% correction capability. It can correct random errors of 3 bits with 100% correction capability and up to 7 random errors with a correction capability of 90.64 %. In future work, this technique can be introduced at the network layer or application layer instead of the data link layer of the NoC.

CONFLICT OF INTEREST

The authors declared no conflict of interest is there for the publication of this work.

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