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Evaluating the impact of cluster parameters on FPGA performance and density

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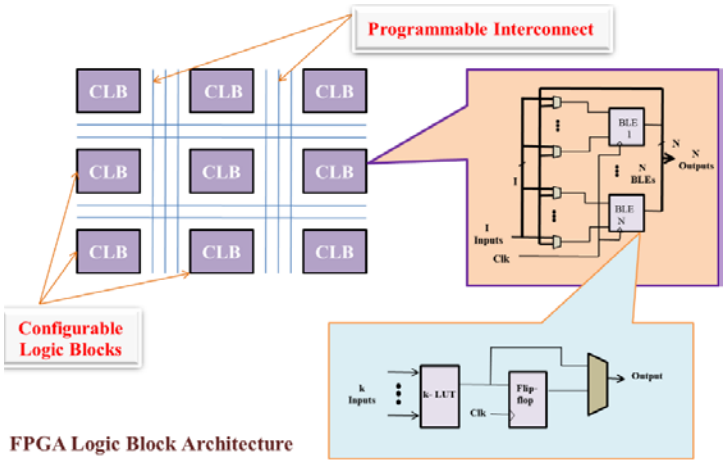
ABSTRACT

There has been a lot of preliminary investigation on the cluster-based Field Programmable Gate Arrays (FPGAs) to determine the cluster parameters that result in an efficient architecture in terms of area or speed or both. However, the advancement of technology and Computer Aided Design (CAD) tools provides numerous reasons to further explore FPGA clusters for possible improvements. This work investigates the area and speed performance of FPGA logic block architectures comprising clusters based on look-up tables (LUTs). Two crucial parameters of the cluster-based FPGA architectures are considered for investigation: the size of LUT (K) and the total inputs provided to a cluster (I). The LUT size is varied from 4 to 7 and the cluster inputs are varied from 40% of the total cluster inputs to their maximum permissible value. Experimentally, using VTR tool flow, it is found that the best area-delay trade-off is obtained for 4-input LUT based cluster using 80% of the maximum cluster inputs. It has been observed that some clusters exhibit better trade-off between area and delay with 70-80% of the total cluster inputs.



FPGA Logic Block Architecture

Keywords: Look-up table (LUT), logic cluster, basic logic element (BLE), CAD, field programmable gate array (FPGA), cluster inputs.

INTRODUCTION

Field Programmable Gate Arrays (FPGAs) are being used in innumerous applications owing to their programmability. The lower cost and faster time-to-market have led to the widespread use of FPGAs in several fields. P. Babu et. al.[1] illustrated FPGA recofigurable architecture, its types as well as different application areas in detail. Notably, some areas where FPGAs are being increasingly used include wireless communication systems,[2] embedded systems,[3] medical imaging,[4] consumer electronics[5] and digital signal processing.[6] Recently, FPGAs are also being employed for the implementation of neural networks,[7] encryption algorithms[8] to ensure data security, among others. However, FPGAs have lower area-efficiency and speed in comparison to Application –specific integrated circuits (ASICs).[9] There is a need to reduce this performance gap in order to boost the utility of FPGAs. FPGA designers aim to lower this gap by careful selection of the logic elements since the performance of a given circuit implemented in an FPGA is strongly influenced by the design of its logic block architecture.

Earlier published works on FPGA logic block architectures[10–14] were primarily based on homogeneous logic elements. Nearly all the commercial FPGAs used look-up tables (LUTs) as the logic element due to their flexibility. However, there is an exponential increase in the area of LUTs with the number of inputs. Therefore, it is not desirable to use LUTs with larger number of inputs. In order to create a larger logic block, some similar LUTs can be grouped together to form a logic cluster.[15] Such logic cluster based architectures are the focal point of investigation in the present research study. In cluster-based FPGAs, a logic block includes a group of basic logic elements (BLEs) connected by high-speed local interconnect. A cluster is usually defined using the given parameters:

1. LUT size (k): represents total inputs to a LUT.
2. Cluster size (N): represents total BLEs in a cluster.
3. Cluster inputs (I): represents total inputs to a cluster.

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Most of the preliminary research studies on cluster-based FPGAs[15–21] have been conducted more than a decade ago. However, there has been a rapid advancement in technology as well as CAD tools. Hence, there is a need to further explore FPGA clusters using latest CAD tools. This research work investigates the effect of two cluster parameters, k and I on the FPGA speed and area.

ARCHITECTURE

This work focuses on the FPGA architectures comprising logic clusters surrounded by programmable interconnect. Each logic cluster is composed of more than one Basic Logic Element (BLE). As demonstrated in Figure 1, a BLE is made up of a k-input LUT and a flip-flop. Figure 2 shows how N BLEs are interconnected to form a logic cluster. The size of the cluster, N is determined by the number of BLEs in a logic block. In a size N cluster consisting of k-input LUTs, the total number of BLE inputs are k.N. Each logic cluster is provided with I external inputs. The cluster as shown in Figure 2 is fully connected; i.e. the multiplexers connect k.N BLE inputs to any of the inputs, I or outputs, N.

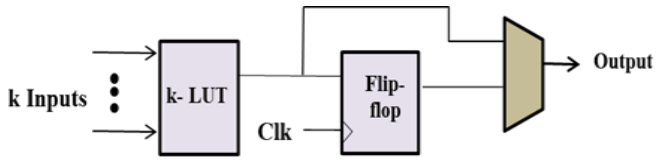

Figure 1: General Basic logic element (BLE) structure.

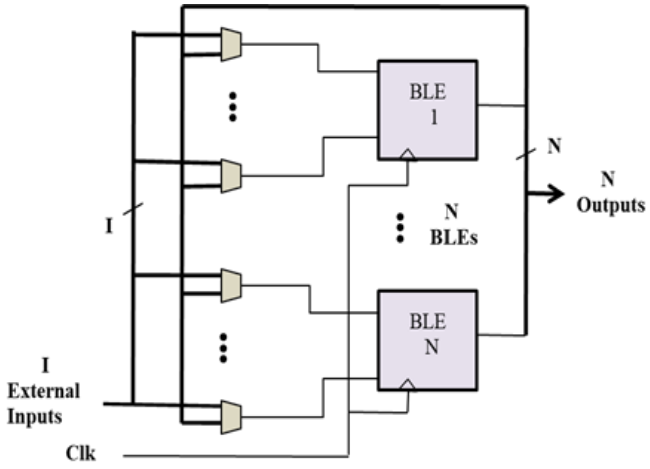

Figure 2: General Logic cluster structure.

RELATED WORK

As earlier discussed, the prior published studies[10–14] were based on the use of homogeneous or identical logic elements. The study[10] was based on an arbitrary combinational logic block whereas the research work[11] used a k-input LUT based logic block for investigation. It was found that the block which provides a higher functionality will result in a more area-effcient architecture. Experimental results indicated that the LUTs with 3 or 4 inputs are the most area-efficient.[11] Subsequent research studies[12–14] focused on the FPGA speed performance. S. Singh et. al.[12] found that 4-input and 5-input LUTs, wide-input PLA-style AND-OR gates and the Actel logic block are almost equivalent in respect of delay measures. The research study[13] evaluated the impact of cell granularity on the FPGA performance. Experimentally, it was found that a cell with 4 or 5 inputs yields the best delay results. Further research work[14] used an experimental approach to investigate the effect of four different classes of logic elements on the FPGA speed. 5- and 6-input LUTs were found to exhibit good performance with the lowest delay values.

To summarize, LUTs with 4 inputs are good in terms of area and LUTs with 5 or 6 inputs are superior with regard to speed performance. In order to implement more logic functionality, LUTs with larger inputs can be used. As a result, fewer logic blocks will be required for the implementation of a given circuit. However, there is an exponential increase in the LUT complexity with the number of inputs. Hence, rather than using a logic blok with larger-input LUT, various LUTs can be simply grouped together using local routing to form a cluster. Such cluster-based FPGAs were investigated[15–22] to determine the optimum cluster parameters.

The research study[16] evaluated the area of FPGA architectures using clusters of distinct sizes (by varying N) and with different cluster inputs (by varying I). The logic clusters based on 4-input LUTs were used for investigation. Related work by V. Betz and J. Rose[15] also investigated the impact of cluster size, N as well as cluster inputs, I on the FPGA area-efficiency. In addition, it was shown that the routing flexibility of FPGA should be reduced as the size of logic cluster is increased.

Relative to the prior studies[15,16] which evaluated only the area measures of logic clusters, the research work[17] investigated the speed as well as area-efficiency of clusters of varying sizes in an FPGA. The best size of logic cluster was determined using area-delay product as the evaluation metric. For all the experiments, the relation I = 2N + 2 was used.

Subsequent study[18] investigated the impact of size of cluster on the speed and area of FPGA as well as on the design compile time, using a timing driven CAD flow. Further, the impact of LUT size (K) as well as size of cluster (N) on the area and delay of an FPGA was investigated in earlier reports.[19,20] I. Kuon et. al.[21] determined the area-delay trade-offs when the architecture as well as transistor sizing of an FPGA were varied. The research study[22] re-evaluated the effect of several cluster parameters on the FPGA performance with latest CAD tools, in a 65 nm technology.

In the past, there has not been much exploration of the impact of cluster inputs on the FPGA area and speed. The present work will examine the effect of varying cluster inputs on the FPGA performance for different sizes of LUT.

EXPERIMENTAL METHODOLOGY

This study aims to determine the k and I values that provide the best feasible trade-off between delay and area. The area and speed of each FPGA implementation is computed experimentally by using a set of MCNC benchmark circuits. The methodology involves technology mapping followed by placement and routing of the benchmark circuits into each architecture using VTR CAD flow to figure out the area and speed measures.

CAD Flow:

The experimental CAD flow is illustrated in Figure 3. The benchmark circuit and architecture description file[23] are given as inputs to the CAD flow. ODIN II[24] is used to perform elaboration and partial synthesis of the Verilog code in order to create a netlist comprising the structures available, as represented in the given architecture file. This netlist output is further passed to the ABC tool for logic optimization followed by technology mapping of the soft logic into the lookup tables (LUTs) and flip-flops. Further, VPR is used to perform packing, placement and routing of the circuit. Finally, the delay as well as area estimation to determine the circuit performance is done using VPR.

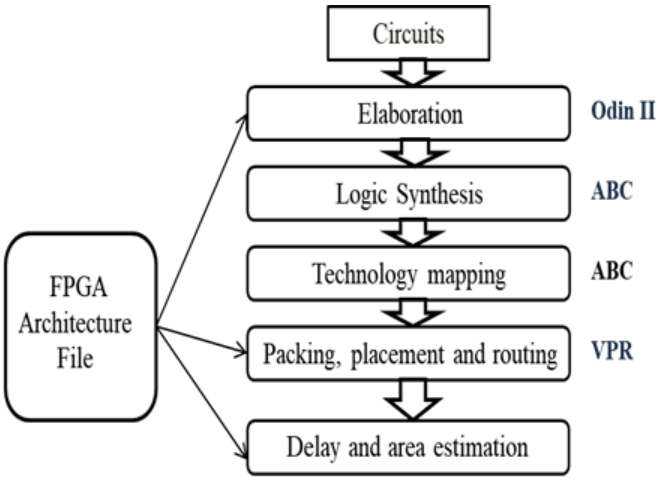

Figure 3: CAD flow.

RESULTS AND DISCUSSION

As earlier discussed, we wish to determine the number of cluster inputs, I which are required in a cluster to obtain better area-delay results. To do so, the critical path delay as well as total area of various FPGA architectures is compared using VTR 7.0[25] in 40nm technology. An important metric for evaluating FPGA architectures is area-delay product.[17] The architecture with the minimum value of area-delay product is considered good as it indicates that smallest amount of area is sacrificed for the maximum gain in performance or vice-versa. The careful selection of FPGA cluster parameters is must to have a good area-delay trade-off.

Effect of varying cluster inputs on total area of clusters using LUTs of different sizes

The research studies[15,16] determined the number of external inputs, I required in order to achieve 98% logic utilization, but did not consider the effect of cluster inputs on the FPGA area and performance. In the present work, we will investigate the impact of varying I on FPGA area and performance. To do so, the cluster inputs are varied from 40% of maximum cluster inputs to their maximum value.

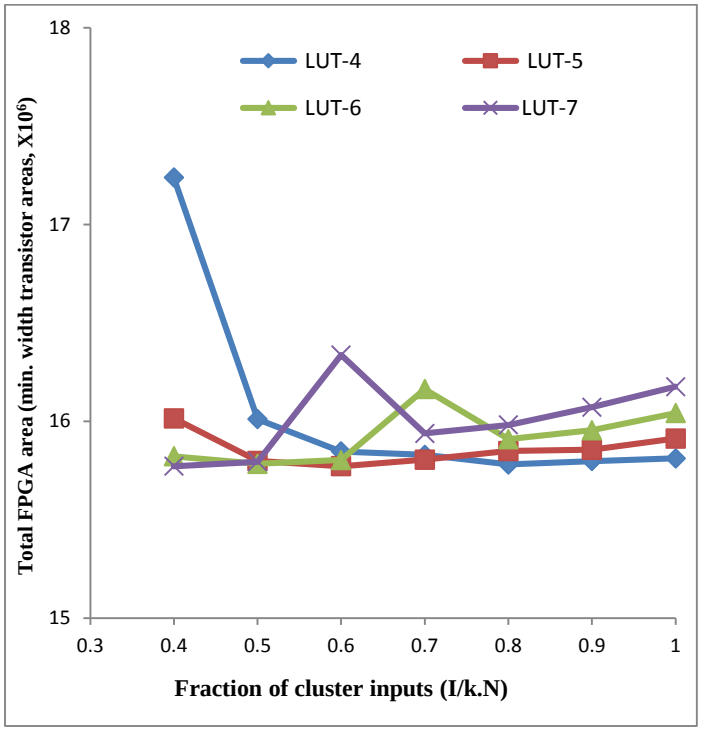

Figure 4: Total FPGA area vs. fraction of cluster inputs.

Here, we will examine the number of minimum cluster inputs required for a LUT-based cluster to achieve good area-efficiency. Since the number of transistors which are needed for multiplexers shown in figure 2 grows linearly with the cluster inputs (I), so I should be chosen as low as possible. On the other hand, if I is chosen to be too small, then it will reduce the logic utilization because many BLEs become unusable.[15,16] Therefore, we will identify the value of I that results in an area-efficient architecture by running MCNC benchmark circuits through the CAD flow shown in figure 3.

In Figure 4, the variation of geometric average of total area of FPGA with cluster inputs for four different LUT sizes is shown. Usually, the value of I is taken between 50 and 60% of highest possible BLE inputs so as to achieve 98% logic utilization. As seen in the graph, the area results are also reasonably good at approximately 50% of the maximum possible cluster inputs, for all LUT sizes. Hence, 50 to 60% cluster inputs are sufficient to achieve good area-efficiency.

Effect of varying cluster inputs on critical path delay of clusters using LUTs of different sizes

Figure 5 shows how the geometric average of the critical path delay varies with the fraction of cluster inputs. The graph indicates that when we use 70-80% of the highest feasible BLE inputs i.e. I = k X N, there is an improvement in the critical path delay, for some LUT sizes. As suggested by earlier research studies, the cluster inputs are chosen between 50-60% of the maximum cluster inputs but, the results here indicate that adding some more inputs to a cluster can result in improved performance for some LUT sizes.

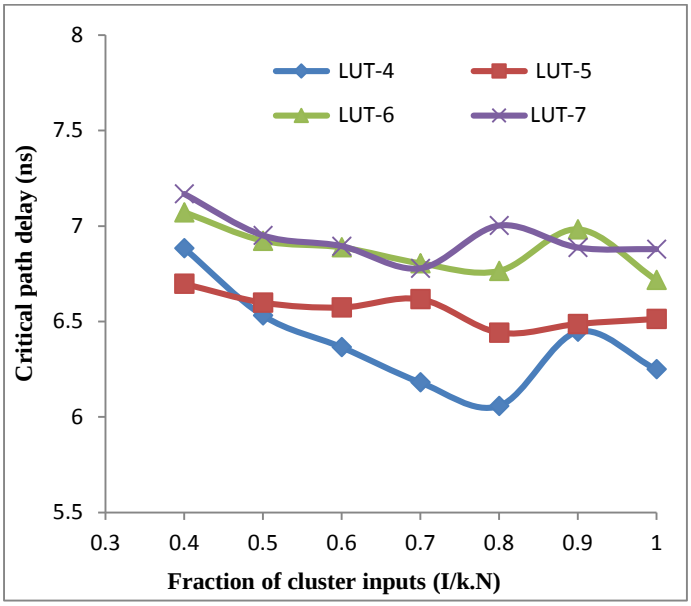

Figure 5: Total critical path delay vs. fraction of cluster inputs.

Effect of varying cluster inputs on area-delay trade-off of clusters using LUTs of different sizes

Figure 6 shows the variation of the geometric average of area-delay product with the fraction of cluster inputs. As we can see in the graph, for small LUT sizes 4 to 6, the minimum value of area-delay product is obtained around 80% of the cluster inputs whereas for LUT-7, the minimum value is achieved when we use 70% of the total inputs. Since area-delay product is chosen as the metric to assess the quality of FPGA architectures, so the results in the graph indicate that using LUT clusters with inputs ranging between 70-80% of the maximum possible cluster inputs can result in the better area-delay trade-off. The best area-delay results are obtained for LUT-4 based cluster with 80% of the highest permissible cluster inputs.

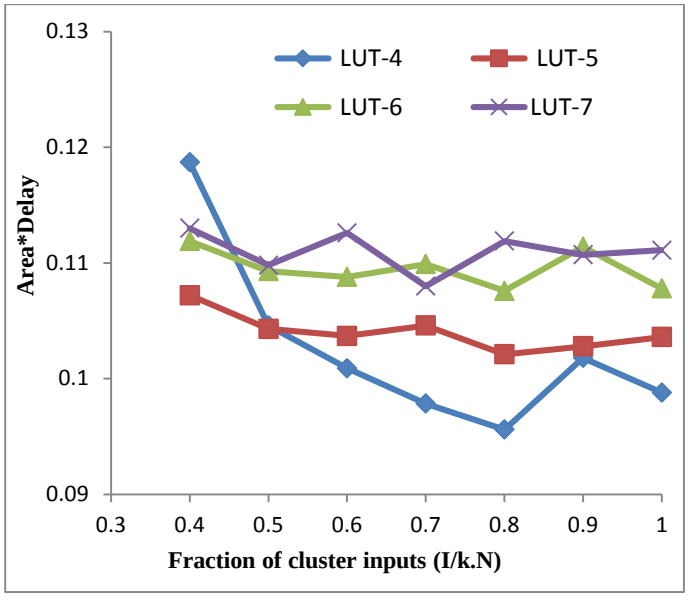

Figure 6: Area-delay product vs. fraction of cluster inputs.

Conclusion

Area and speed are two key metrics for FPGAs. In this work, the effect of logic cluster inputs on the FPGA area and performance was examined for different LUT sizes using VTR CAD flow. An FPGA cluster with suitable values of k and I will result in an efficient architecture. The exploration of several architectures indicates that some LUT clusters show better area-delay trade-off when cluster inputs are chosen between 70-80% of their maximum value. Specifically, it is found that 4-input LUT based cluster with 80% of total BLE inputs provides the best area-delay results.

Abbreviations

FPGA: Field-programmable gate array
CAD: Computer-aided design
LUT: Look-up table
ASIC: Application-specific integrated circuit
BLE: Basic logic element

Conflict of Interest Statement

Authors have no conflict of interest.

References

1. P. Babu, E. Parthasarathy. Reconfigurable FPGA Architectures: A Survey and Applications. *J. Inst. Eng. India Ser. B* **2021**, 102 (1), 143–156.
2. J. Lorandel, J.-C. Prevotet, M. Helard. Fast Power and Performance Evaluation of FPGA-Based Wireless Communication Systems. *IEEE Access* **2016**, 4, 2005–2018.
3. S. Perri, F. Frustaci, F. Spagnolo, P. Corsonello. Design of Real-Time FPGA-based Embedded System for Stereo Vision. In *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*; IEEE, Florence, **2018**; pp 1–5.
4. G.D. Licciardo, C. Cappetta, L. Di Benedetto. Design of a Gabor Filter HW Accelerator for Applications in Medical Imaging. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2018**, 8 (7), 1187–1194.
5. H. Taghipour, J. Frounchi, M.H. Zarifi. Design and implementation of MP3 decoder using partial dynamic reconfiguration on Virtex-4 FPGAs. In *2008 International Conference on Computer and Communication Engineering*; IEEE, Kuala Lumpur, Malaysia, **2008**; pp 683–686.
6. K. Sano, S. Yamamoto. FPGA-Based Scalable and Power-Efficient Fluid Simulation using Floating-Point DSP Blocks. *IEEE Trans. Parallel Distrib. Syst.* **2017**, 28 (10), 2823–2837.
7. S.S. Lingala, S. Bedekar, P. Tyagi, P. Saha, P. Shahane. FPGA Based Implementation of Neural Network. In *2022 International Conference on Advances in Computing, Communication and Applied Informatics (ACCAI)*; IEEE, Chennai, India, **2022**; pp 1–5.
8. S. Sanap, V. More. Field Programmable Gate Array (FPGA) based implementation of efficient RC6 block cipher. *J. Integr. Sci. Technol.* **2022**, 10 (2), 168–172.
9. I. Kuon, R. Jonathan. Measuring the Gap Between FPGAs and ASICs. *IEEE Trans. Comput.-AIDED Des. Integr. CIRCUITS Syst.* **2007**, 26 (2).
10. J. Rose, R.J. Francis, P. Chow, D. Lewis. The effect of logic block complexity on area of programmable gate arrays. In *1989 Proceedings of the IEEE Custom Integrated Circuits Conference*; IEEE, San Diego, CA, USA, **1989**; p 5.3/1-5.3/5.
11. J. Rose, R.J. Francis, D. Lewis, P. Chow. Architecture of field-programmable gate arrays: the effect of logic block functionality on area efficiency. *IEEE J. Solid-State Circuits* **1990**, 25 (5), 1217–1225.
12. S. Singh, R. Jonathan, L. David, C. Kevin, C. Paul. Optimization of field-programmable gate array logic block architecture for speed. In *Proceedings of the IEEE 1991 Custom Integrated Circuits Conference*; IEEE, San Diego, CA, USA, **1991**.
13. J.L. Kouloheris, A. El Gamal. FPGA performance versus cell granularity. In *Proceedings of the IEEE 1991 Custom Integrated Circuits Conference*; IEEE, San Diego, CA, USA, **1991**; p 6.2/1-6.2/4.
14. S. Singh, J. Rose, P. Chow, D. Lewis. The effect of logic block architecture on FPGA performance. *IEEE J. Solid-State Circuits* **1992**, 27 (3), 281–287.

15. V. Betz, J. Rose. How much logic should go in an FPGA logic block. *IEEE Des. Test Comput.* **1998**, 15 (1), 10–15.
16. V. Betz, J. Rose. Cluster-based logic blocks for FPGAs: area-efficiency vs. input sharing and size. In *Proceedings of CICC 97 - Custom Integrated Circuits Conference*; IEEE, Santa Clara, CA, USA, **1997**; pp 551–554.
17. A. (Sandy) Marquardt, V. Betz, J. Rose. Using cluster-based logic blocks and timing-driven packing to improve FPGA speed and density. In *Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays*; ACM, Monterey California USA, **1999**; pp 37–46.
18. A. Marquardt, V. Betz, J. Rose. Speed and area tradeoffs in cluster-based FPGA architectures. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2000**, 8 (1), 84–93.
19. E. Ahmed. The effect of logic block granularity on deep-submicron FPGA performance and density. Thesis, University of Toronto, University of Toronto.
20. E. Ahmed, J. Rose. The effect of LUT and cluster size on deep-submiron FPGA performance and density. *IEEE Trans. Very Large Scale Integr. VLSI Syst.* **2004**, 12 (3), 288–298.
21. I. Kuon, J. Rose. Area and delay trade-offs in the circuit and architecture design of FPGAs. In *Proceedings of the 16th international ACM/SIGDA symposium on Field programmable gate arrays*; ACM, Monterey California USA, **2008**; pp 149–158.
22. G. Zgheib, P. Ienne. Evaluating FPGA clusters under wide ranges of design parameters. In *2017 27th International Conference on Field Programmable Logic and Applications (FPL)*; IEEE, Ghent, Belgium, **2017**; pp 1–8.
23. J. Luu, J.H. Anderson, J.S. Rose. Architecture description and packing for logic blocks with hierarchy, modes and complex interconnect. In *Proceedings of the 19th ACM/SIGDA international symposium on Field programmable gate arrays*; ACM, Monterey CA USA, **2011**; pp 227–236.
24. P. Jamieson, K.B. Kent, F. Gharibian, L. Shannon. Odin II - An Open-Source Verilog HDL Synthesis Tool for CAD Research. In *2010 18th IEEE Annual International Symposium on Field-Programmable Custom Computing Machines*; IEEE, Charlotte, NC, USA, **2010**; pp 149–156.
25. J. Luu, J. Goeders, M. Wainberg, et al. VTR 7.0: Next Generation Architecture and CAD System for FPGAs. *ACM Trans. Reconfigurable Technol. Syst.* **2014**, 7 (2), 1–30.