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Distinct ρ-based DGMOSFET Low Power circuit for stable read and write CAM cell

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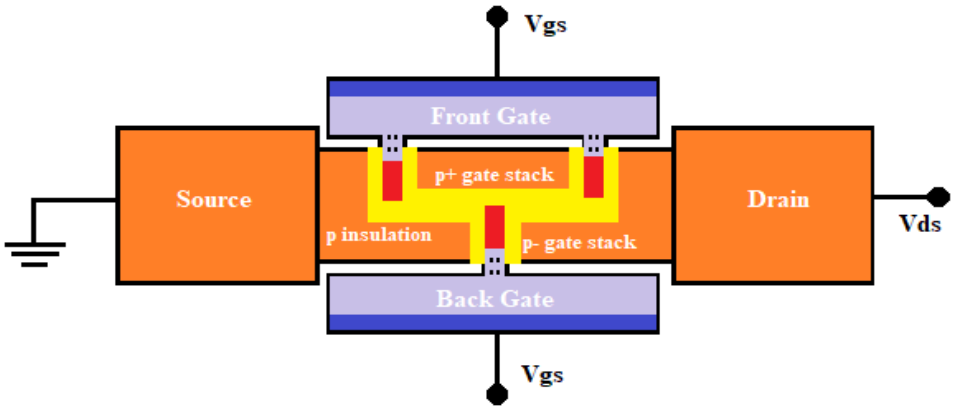
ABSTRACT



In recent research works, content-addressable memory (CAM) has become an important device design for high-speed in-memory search for pattern-matching operations by searching memory data with stored content in memory locations in one cycle of memory read, rather than finding the stored memory content through data address. Such CAM circuit designs remain a challenge in consuming high power, as the CAM cell circuit suffers from sharing of short circuit current path and charge stored across the short circuit match-line (ML). In recent literature, MOSFET-based CAM designs suffer from a delay in ML search and utilize high power in the charge control circuit. In the proposed work, through a distinct ρ-based DGMOSFET device a ballistic transport mobility equation is described to estimate the ML short circuit current path and charge as a consequence of low power static and transient performances at CAM cell circuit level to stabilize the content during read and write operation to limit the search delay in ML and device power consumption. The proposed model is simulated using 90-nm-technology and comparative results show proposed low-power-CAM-cell circuit through Distinct ρ-based DGMOSFET device limits the sharing of short circuit current path and charge by reducing power consumption effectively.

Keywords: low power CAM, search delay, ballistic transport, short-channel effects, DIBL

INTRODUCTION

Multi-gate MOSFETs continue to shrink at a greater rate; the physical ballistic transport is considered during the simulation of the device model. The double-gate MOSFETs (DGMOSFETs) which are designed with nanometer scale channel lengths are having more ballistic compared to diffusive ones. For this nanometer scale, a compact model has to be developed to change from drift-diffusion to ballistic region. The impact of ballistic and quasi-ballistic transport has to be evaluated at the DGMOSFET circuit level. In our recent work[1] on the design of a distinct ρ-based DGMOSFET device, the doping levels of the left-and-right front with back gate are varied with surface regions through reducing dielectric layer potential changes to analyze the junction capacitances variations, which makes the sub-threshold value to reduce. This paper method adopts a distinct ρ-based DGMOSFET device, to design a CAM cell circuit for read-and-write analysis.

During CAM cell content search to find the matched line in a table and to analyze the number of memory words a possibility of usage for a priority encoder. This search operation requires a lookup operation to increase the speed of CAM. But there is a tradeoff between the speed of CAM and power consumption with device silicon area.[2] Distinct ρ-based DGMOSFET can improve the drive current by reducing the short channel effects (SCE) that affect

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I-V device values and control drain-induced barrier lowering (DIBL) by scaling the MOS device to limit device power consumption.[3] To make use of [1] in this proposed work, a shorted gate method is used, in which the distinct ρ-gates are reduced with the length parameter to give an improved current drive.

From the literature survey works,[4] in this paper authors have implemented a ballistic and quasi-ballistic transport mechanism to form a drift-diffusion in CAM circuit design through.[1] Using this approach, a thorough analysis is made which impact the performance of the CAM circuit based on DGMOSFET devices.[5]

LITERATURE REVIEW

Earlier works have shown an improvement in drain current during the ballistic transport operation on the MOSFET device.[6] And its usage is qualitatively demonstrated,[7] where a flux-based ballistic transport operation is defined, which has improved performance drain current. The main usage of methods[8] is in devices with physical thickness is less in terms of mean free path, providing a predominant usage of quasi-ballistic transport.[9] In ballistic transport described through drift-diffusion relationship, which describes a transport model through Boltzmann transport equation can estimate the ballistic transport.[10]

The conventional CMOS based CAMs are analyzed, which are having a lower density than SRAMs, which made a limitation in manufacturing high-capacity memory with existing CMOS-based CAMs,[11] because of having the high power-consumption problem. CAM architectures with high-speed are studied. In CAM cell circuit design, each CAM word if having a single match-line (ML), before the operation of search; now the device MLs were at high voltage through pre-charged, in content-search operation, search-word is matched with single content word and it holds the charge.[12] And the remaining mismatched MLs are discharged. These cycles of high voltage pre-charging and discharging of MLs continue to consume dynamic power in the CAM cell. In reported stuides,[13] segment-based word architecture is proposed for power-consumption-reduction by switching the power. Dynamic ML power consumption is reduced by the pre-computation method. A pre-charge-free CAM is developed to reduce the short circuit current path when MLs are in mismatch condition. In the output, power consumption is controlled based on a self-controlled pre-charge design. CAM designs[14] are primarily focused on priority encoders to reduce power in CAM cell array and ML sense. In CAM cell used the “resolve-then-encode” method through Multiple Match Resolution (MMR) and Address Encoding (AE). The MMR has based on MLs critical and non-critical paths, which created huge loads on CAM cell clock drivers.[10]

The designs illustrated above are developed to improve performance,[15] but the static and dynamic power consumptions are not limited. In this paper, to overcome the drawback of CAM cell design in power consumption, a new DGMOSFT model for low power pre-charge-discharge-computation based CAM ML architecture is designed, in which the pre-discharge control is based on the charge variations at neighbor CAM cell ML nodes.[9,16]

Among MOSFETs, the symmetrical DGMOSFET in planar forms performs better characteristics for short-channel effect (SCE) immunity, channel electrostatics, and channel length scaling.[17] The channel length scaling for planar DGMOSFETs is made by reducing the channel thickness and oxide thickness.[18] This reduction in channel thickness affects the Quantum Confinement (QC), which impacts the electrostatics of the channel thickness and channel length scalability with the defined channel structure.[19] With this reduce in gate control over the channel by the drain current variations, at a very short channel length; there is a further increase in QC effects. As the QC effect increases, further reducing the thickness of the channel and oxide is not sufficient to have better gate control over the channel and so there is a need for a better solution for high scalable channel length for an improved DG MOSFET. To meet better channel electrostatic parameters like sub-threshold slope and threshold voltage, there is a need for short channel DG MOSFET design over a scalable channel and oxide thickness in effects to QC.

The structure of DG MOSFET considering the size of the device is an important parameter for performance and power output. A DG MOSFET, defined as a dual-gate device with side walls extended into the buried oxide has an easier fabrication of dual-gate MOSFET than single-gate MOSFET.[20] With the dual-gate channel electrostatic variations, the short-channel effects were controlled and doping of the channel with the body can be simulated through separate bias gate voltages.[21] When impact ionization occurs with an elevating value than junction-less-devices, then drain voltage is controlled to obtain a better sub-threshold slope.[22] With the change in threshold voltage and drain-induced barrier lowering, the high dielectric constant material is made useful for gate oxide of the double-gate MOSFET analyzed. From these, we can say that through a high-k material for gate-oxide the threshold voltage is increased with a reduction in change between channel size and oxide thickness. And there is an increase in drain-on-off ratio currents with an improved subthreshold slope,[23] by this, we can attain a better trans-conductance through output conductance and intrinsic gain having a low gate voltage for suitable gate layers.[24]

Another way of approximate search CAMs uses high-sensitivity hashing of stored data and query patterns. With these approaches for large data capacity and search, the data does not make a low similarity of CAM data.[25,26] CAM design for a minimum search through digital circuitry for bit storage and comparison also takes a better functionality in search operation.[27] In n-bit CAM cell,[28] near-memory logic is designed to calculate the sum of squares of CAM data word for data vectors similarity differences. In versatile CAM cell,[29] the similarity between search operations makes the gates outputs of CAM bit-cells of a word to perform search and store operations. In a report,[30] an approximate search CAMs design uses the speed of match-line discharge as a measure of search distance. In small Hamming distance,[31] is designed through a meticulous timing of the match-line discharge through energy efficient GPUs in an approximate search enables CAM designs. In hamming distance search CAMs, every time a bit mismatch occurs where the score signal is delayed, the Hamming distance between the search and stored patterns is proportional to the delay of the score signal.[32]

From the above comparisons with similar studies discussions, the author(s) have concluded to design a high-k dielectric material based distinct ρ-Based DGMOSFET CAM cell to overcome the above said limitation in conventional CAM cell design.

To summarize, this work analyzed and outlines the following contributions:

- Distinct ρ-Based DGMOSFET CAM cells have a match, mismatch, and approximate search designs using match-line ρ-elements as a measure of SL and ML.
- Distinct ρ-Based DGMOSFET CAM cells have a large pattern search with very high sensitivity to improve sub-threshold slope and limit energy consumption.

MODEL OF DISTINCT P (RHO)-BASED DGMOSFET CAM CELL AND ITS METHODOLOGY-ANALYSIS

As in DGMOSFETs architecture, the available high-permittivity dielectrics materials can provide good control of short-channel effects with higher channel conductivity. But the introduction of these materials at the gate stack causes problems that impact the electrostatic effects of the device. When the gate stack dielectric length is the same as the total gate length and there is a fixed charge at the gate stack, the electrostatic effect of the device becomes severe. The effect of gate stack parasitic charge on induced-barrier-lowering is implemented in ref [1] through a distinct ρ-based DGMOSFET device. To this extent, in this paper, a realistic analysis of a distinct ρ-based DGMOSFET device with crystallized high permittivity materials in the form of crystalline grains are place vertical to a device and charged grain boundaries are generated in a high permittivity layer. These crystalline grains across vertical and at boundaries are induced in the gate stacks across the front-gate stack and back-gate stack. This model approach is a varying crystalline grain length with device verticals and charged device grain boundaries. A varying charge density is analyzed for each grain boundary length variation by a varying vertical device cross-section area, analyzing as a varying charge density by device unit length across vertical and boundary directions from distinct ρ-based DGMOSFET ρ-front gate varying from 1u to 9u and ρ-back gate varying from 4u to 6u, where u=1.28×10^{-12} C/cm.

This research work aims to extend our[1] investigations to the distinct ρ-based DGMOSFET with distributed-and-varied channel length across the doping levels of the left-and-right front with back gate for improving parasitic effect charges on the device sub-threshold response.

A. DISTINCT P (RHO)-BASED LOW POWER DGMOSFET DEVICE-MODEL-STRUCTURE AND PARAMETERS

A symmetrical DGMOSFET with 20 nm –thick Ge film is included with a charge element across a gate causing the device asymmetrical in the high dielectric material. This makes the threshold voltage shift due to the quantum effects for asymmetric DGMOSFETs with 20 nm thick film should not exceed 75 mV. For carrier transport, the channel lengths of 30 nm are considered for ballistic transport is minimized and a drift-diffusion approach to have improved accuracy. The non-stationary ballistic transport impacts the threshold drain current for short gate length values assigned for the front gate and back gate. The drift-diffusion approach provides an efficient subthreshold value at off-state current and subthreshold slope, this analytical approach is showing an accurate SCE behavior in the proposed model design.

In the proposed analytical approach, quantum analysis in the channel is made across the device's vertical direction at a high electric field which is perpendicular to the silicon-oxide layer. Across the device boundary, a quantum simulation is analyzed to take the separation of the amount of charge density at different state changes across the defined sub-bands and conduction band regime.

The quantum analysis is realized for strained silicon channels during vertical scale and on settled SiGe substrates to improve low-power device characteristics and make use of device mobility at high frequency. With the few nanometers thickness of the strained silicon layer, there is significant variation in quantum analytics of ballistic electrons mobility in the channel. This large electron mobility in strained silicon provides a comparable advantage in improving high frequency. From this point of view, considering equilibrium transport and quantum effects, the density gradient approach with a drift-diffusion model is analyzed with the proposed work.

B. DISTINCT P (RHO)-BASED DEVICE CALIBRATION MODEL

The applicable features of our earlier work[1] are having better SCEs, higher I_{on}, etc., for example, as shown in Figure 1, the device characteristics are gate length (L_g) of 22 nm, and distinct ρ-thickness (t_{Si}) of 20-30nm, DIBL is 42m V/V with subthreshold-slope of S ~80m V/decade. Through this, an improved SCEs observed with L_g/t_{Si} ~1 are simulated from a device-physics perspective: which shows a solution of potential energy having a better SCEs with DIBL < 120mV/V, S < 100mV/decade, with better effective channel length (L_{eff}) than t_{Si} value. In this design L_{eff}=L_g, with the gate-induced variations of device characteristics, the switching characteristics are improved. From the device-Si characteristics, with L_{eff} < L_g and with the overlaps of source/drain dopants inside the channel, the simulated structure of the proposed device shown in Figure 1, implies some novel features of [1], with the provided relation between L_{eff} and L_g.

From the above design parameters, the integrated channel charge includes bulk inversion, which is used to calculate the drain current through the height of the device (h_{Si}), which is commonly 2h_{Si}, because the current for each channel is the two factor for two DGMOSFET channels, for drain current bulk inversion analysis.

In analyzing the weak-inversion I_D-V_G device characteristics, the SCEs are considered by the L_{eff}, $t_{Si,}$ and t_{ox}, along with body doping: here L_{eff} is defined as L_{eff}=L_g-Δ_L, where Δ_L is a positive adjacent gate-source/drain overlap. By adjusting the values of device S and DIBL values, SCEs of distinct ρ-device weak-inversion I_D-V_G device characteristics are matched with the off-state current I_{off}. In the DGMOSFET distinct ρ-device structure and its model parameters are evaluated to form the weak-inversion calibration of the linear-region followed by strong-inversion I_D-V_{GS} characteristics.

During low drain bias, the velocity overshoot is reduced causing a self-heating effect, by the strong-inversion the characteristics of the DGMOSFET distinct ρ-device: linear region characteristics, parasitic resistances: drain parasitic resistance (DPR) and source parasitic resistances (SPR) and effective mobility (μ_{eff}) are extracted. But the variations of DPR and SPR can regulate the changes in μ_{eff} and strong-inversion I_D-V_{GS} characteristics, causing the accuracy of these regulated characteristics to reduce, mostly for the short-channel device.

To analyze the calibration parameter, consider the linear region characteristics having total-on-state resistance as R_{ON}, and is expressed as

$$R_{ON} = \frac{V_{DS}}{I_D} = \frac{SPR+DPR}{W} = \frac{L_{eff}}{2\,WC_{of}(V_{GS}-V_t)\mu_{eff}(L_{fm}\theta)} \qquad (1)$$

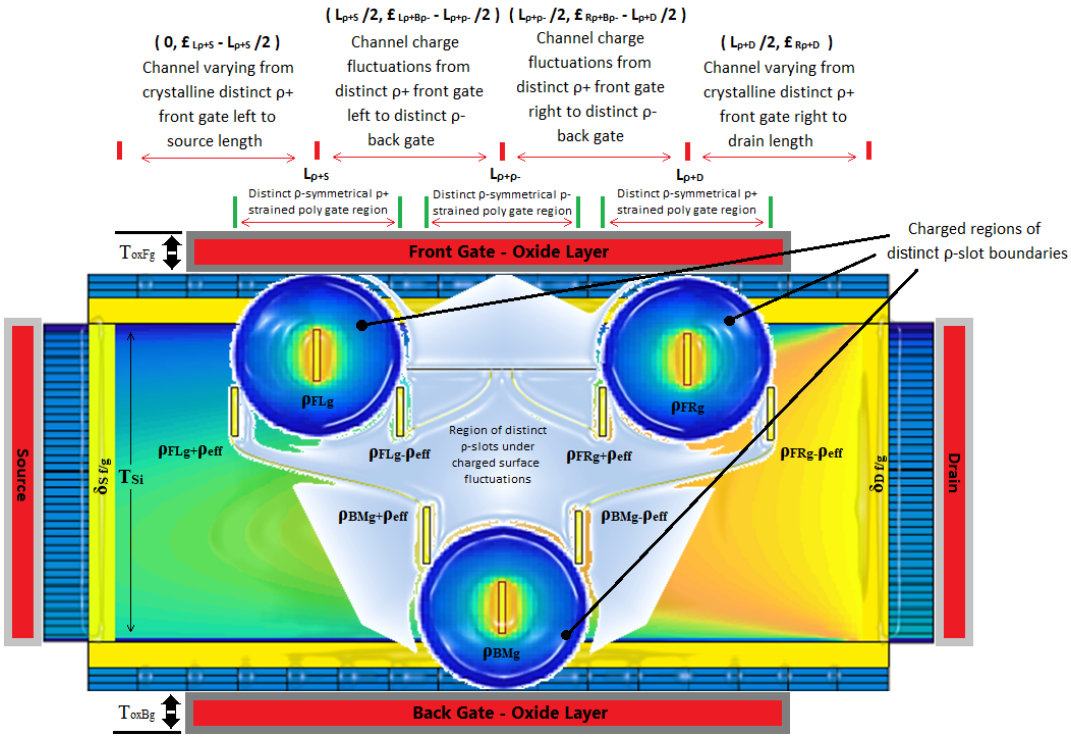


Figure 1 Proposed structure of distinct ρ-based DGMOSFET device calibration model.

where W is width, C_{of} is gate capacitance, V_{GS}: is gate-bias-voltage and V_t: is threshold-voltage, L_{fm}: Low-field mobility for thick TSI (nmos/pmos) and θ is mobility tuning parameter, which is related to a symmetric DGMOSFET analysis.

To limit this drawback in traditional DGMOSFET devices, in the proposed DGMOSFET distinct ρ-device structure, a calibration parameter is introduced which is independent of SPR/ DPR variations. The calibration parameter is related as $g_m/(I_D)^2$, where device on-state resistance is a dependable parameter on g_m.

To calculate the calibration parameter for the ballistic transport equation, differentiate equation (1) for gate bias by assuming the V_{GS} relation as

$$V_{GS} = (V_{GS} - I_D\, SPR/W) \tag{2}$$

And we can observe in (2), that the calibration parameter is independent of SPR/DPR. Through strong-inversion I_D-V_{GS} characteristics at low V_{DS}, the device parameters L_{fm} and θ are adjusted to reach the linear region currently.

With these strong-inversion and saturation-region characteristics, the carrier saturated drift velocity (V_{SAT}) varies iteratively to match I_D-V_D characteristics. Because of the increase in V_{SAT}, the inter-dependent channel current increases, making the difficulty in separating the thermal resistance and capacitance from the effect of velocity-overshoot. This velocity-overshoot makes the proposed DGMOSFET distinct ρ-device structure gain importance in short-channel devices.

In the proposed DGMOSFET distinct ρ-device to limit the velocity-overshoot, a tuning parameter is introduced to reduce the uncertainties caused by quantum mechanical (QM) effects, in device mass, they are effective mass QM parameter (EQM) and effective device QM parameter (DQM). These two parameters EQM and DQM predict the QM effects by solving the Potential energy (PE) and effective-mass Schrödinger equation (SE) self-consistently.

The PE is solved to get the weak-inversion (WI) characteristics by combining them with the drift-diffusion current equation to result in strong-inversion (SI) characteristics. And through the polynomial spline, the moderate-inversion (MI) characteristics are obtained. These polynomial spline coefficients are defined by the physical WI and SI characteristics solutions at MI boundaries. For SI analysis, the use of velocity saturation by incorporating the Boltzmann Transport Equation (BTE) is made.

For SE analysis, the use of a variational method by incorporating device surface effects depends on the device's effective mass and junction valley generation. The device surface effect has transport formalism and a mobility model, which affects different scattering mechanisms, and can be limited by thermal injection, resulting in improved ballistic-like transport.

With the implementation of the above said physical device parameters, the proposed distinct ρ-device becomes an essential device in improving DGMOSFET device and circuit performance.

C. Calibration-Model of Distinct ρ (Rho)-Based DGMOSFET-Device Implementation

Firstly, the calibration model with a distinct ρ-based-device is fabricated to DGMOSFET having L_g=110 nm, having an undoped device body with source-drain stack slots doped by 0^0 tilt ion implantation with gate boundary spacers. The stack slot thickness varies from 20nm to 30nm, and the stack slot extension lengths are

100nm each with gate oxide 20 Å thick poly-Si used for gate material.

For WI calibration, we can obtain subthreshold slope and off-state current by keeping L_{eff}=140nm which is longer than L_g = 40 nm.

For SI calibration, we have to take a high SPR/DPR value, which predicts the saturation-region characteristics with the liner-region current.

For perfect-inversion (PI) calibration, we get two device insights from the calibration effort process. They are: one is that the effective channel length is longer than the physical channel length and the second is that the device resistances across the source and drain are very high. These two device insights are bias-dependent making it possible to keep both linear and saturation-region currents through constant device resistances across the source and drain.

In PI, the increase of gate bias in the linear region causes the SPR/DPR to decrease gradually – as the fact is that the increase of gate bias increases carrier concentration in the device stack slot regions.

In PI, the increase of drain gate in the saturation region causes the SPR/DPR to remain constant – as the fact is that it is a good match and indicates an increase in saturation carrier concentration in the device stack slot regions.

For enough PI, calibration between SPR and DPR is important. During gate bias, only SPR reduces keeping DPR constant. During drain bias both SPR and DPR reduce, as the DPR value increases further – the device channel reaches saturation, where the saturation current remains as an independent parameter of DPR.

These SPR and DPR asymmetric calibrations are limited by a process symmetry method in the proposed calibration model. With this symmetry method, we can make SPR=DPR in all bias regions. In the symmetric method, the uncertainty of device resistances across source and drain magnitudes is due to poly-depletion-induced degradation of asymmetric channel current.

The poly-depletion effect reduces I_D value and increases V_{GS} values, so making an ineffective poly-depletion effect on device resistances across the source and drain magnitudes, the SPR/DPR is to be increased in turn causing the device resistances across the source and drain magnitudes to increase with gate bias. So with this symmetric method, the overlaps occurred in channel formation, and underlap occurred in stack slot formation, the poly-depletion effect could not affect the SPR=DPR calibration, by monitoring the values of SPR/DPR (I_D) and SPR/DPR (V_{GS}) at quantitative margin levels.

The proposed distinct ρ-based DGMOSFET device fabrication implementation is categorized in the presence of overlaps and underlaps as: longer underlap lengths and shorter overlap lengths.

The channel is undoped, an excessive extension doping measures are avoided to limit the punch-through mechanism, to understand the effects of underlaps on distinct ρ-based DGMOSFET device fabrication, we use the 2D numerical TCAD simulator, to simulate the idealized distinct ρ-based DGMOSFET device simulation structure characteristics is illustrated in Figure 2 and Figure 3.

The structure is idealized because the number of source/drain dopants (NSD) across the longer underlap regions (L_{eS}/L_{eD}) becomes zero, as it is a no dopant region and makes the simulation run time with energy quantization effects to turned off. The device structure is considered as having L_g=20nm with t_{oxf}=t_{oxb}=2nm.

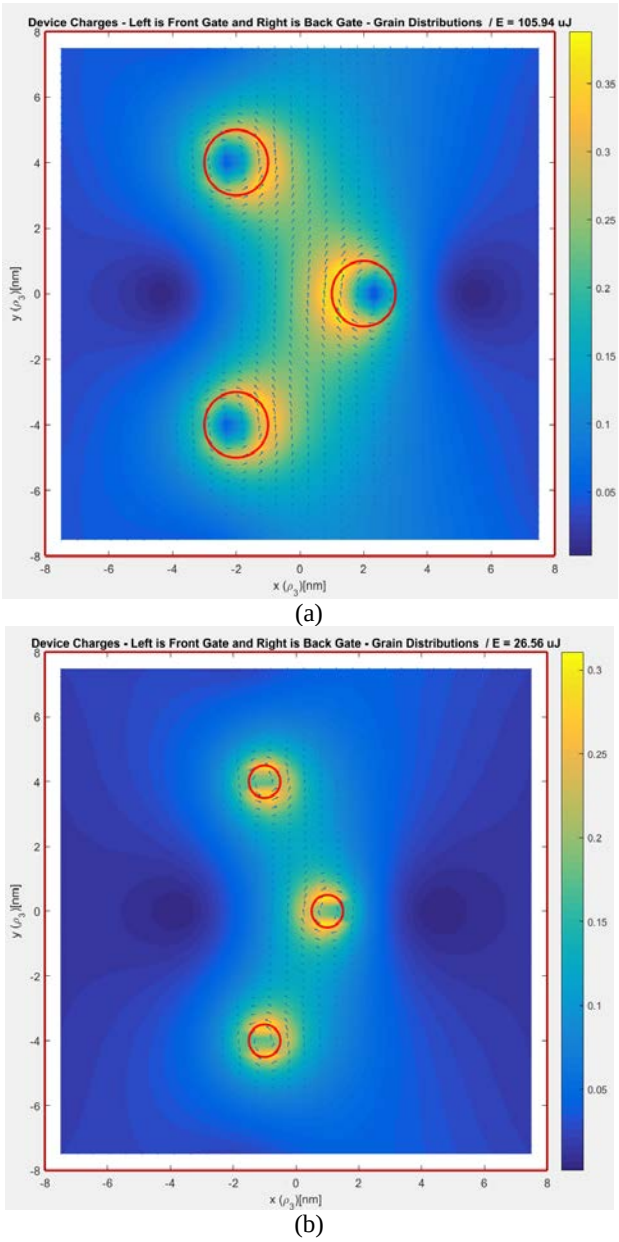


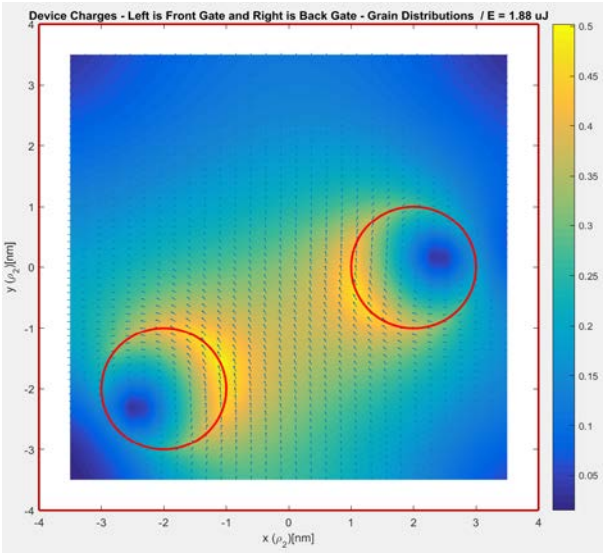
Figure 2 Simulation characteristics of distinct ρ-based DGMOSFET device charges - Left is front gate and right is back gate - grain distributions under longer underlap lengths: (a) Illustration of longer underlap lengths of gate grain positions at equipotential positions and (b) Illustration of longer underlap lengths of gate grain positions at increasing device charge positions.

1) For longer underlap lengths,

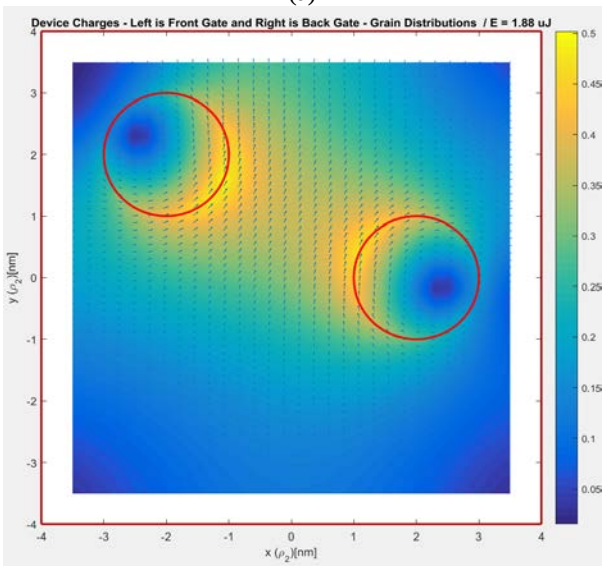
The effects of increasing underlap on subthreshold swing *S* are shown in Figure 2. As we increase the underlap length, the channel effective length increases causing the SCEs and *S* to decrease. And with underlaps, the stack slot thickness is reduced and the decrease of *S* will decrease L_{eS}/L_{eD} to> 10nm. For DIBL, as DIBL varies with $t_{Si}t_{ox}$/$(L_{eff})^2$, any increase in channel effective length reduces the t_{Si} or t_{ox}.

So from t_{Si} and t_{ox} values, we can fabricate a thin film technology reliably. For longer underlap lengths, SCEs relax to L_{eS}/L_{eD} and L_{eff} : which affects the coupling of two gates, which defines the stack

slot thickness to control the SCEs. Hence, for longer underlap lengths *S* the SCEs are relaxed with L_{eS}.



(a)



(b)

Figure 3 Simulation characteristics of distinct ρ-based DGMOSFET Device Charges - Left is Front Gate and Right is Back Gate - Grain Distributions under shorter underlap lengths: (a) Illustration of Shorter overlap lengths of the front left gate and back gate grains position at equipotential positions and (b) Illustration of Shorter overlap lengths front right gate and back gate grains position at equipotential positions

2) For Shorter overlap lengths

The variation of I_{on} and I_{off} with L_{eS}/L_{eD} is considered as shown in Figure 3. Decreasing the overlap lengths increases L_{eff}, which reduces the SCEs and I_{off}. This decrease in overlap lengths increases SPR / DPR and decreases I_{off}.

And with overlaps, the stack slot thickness can be decreased by considering L_{eS}/L_{eD} as < 5nm, causing I_{off} to increase and making the device shorter at 5nm. The shorter overlap lengths increase the resistance causing the relaxation effects on SCEs. For effective DIBL and S variations, the gate stack slots are in the middle with symmetric overlaps on both sides; as DIBL and S are relaxed.

The S variations defined by L_{eff}, do not depend on gate position exactly when we consider the gates nearby the drain/source. And considering zero dopants (NSD) from drain/source increases gate stack controls by creating a shorter overlap length region, which keeps a constant off-state current. The on-state current is available near the gate to the source at a maximum flow of dopants near the drain/source.

Hence, as the dopants are zero with smaller L_{eS}, there is a reduction of effective gate bias through R_{eS} causing the SCEs to relax with L_{eD}.

D. Distinct ρ (Rho)-Based DGMOSFET Device Low Power Analysis

For low-power analysis, through Poisson equations, a general model is implemented and verified by the TCAD simulator. Consider a DGMOSFET. Let denote left-and-right-front gate voltages as V_{gf} and back gate voltages as V_{gb}. Representing the silicon film thickness as t_{si}, the thickness-of-oxide-for-front-gate as t_{of} with thickness-of-oxide-for-back-gate as t_{ob}.

Considering a symmetric DGMOSFET with $t_{of} = t_{ob}$ and natural length scale (λ) is analyzed for SCEs. To relax SCEs, minimum-channel-length is $L_{min} = m\lambda$, where m is based on device usage, and the value of m varies between 5 and 10.

For our analysis, considering the 2D Poisson equation, the solution is obtained as: $\lambda = \sqrt{\beta/[2(1+\alpha)]}$, where

$$\alpha = \frac{\grave{o}_{si}}{\grave{o}_{ox}}\frac{t_{si}}{t_{of}} + \frac{t_{ob}}{t_{of}},\ \beta = 2\frac{\grave{o}_{si}}{\grave{o}_{ox}}t_{ob}t_{si} + t_{si}^2.$$

This results in two conditions: 1) for DGMOSFET considering $t_{ob}\approx\infty$, $\lambda = \sqrt{(\grave{o}_{si}/\grave{o}_{ox})t_{of}t_{si}}$ and 2) for symmetrical DGMOSFET considering $t_{ob}=t_{of}$, $\lambda = \sqrt{(\grave{o}_{si}/2\grave{o}_{ox})t_{of}t_{si}}$.

From these two conditions, the length scales of these at different t_{of} and t_{si} are given in Table 1.

Table 1: DOMOSFET length-scales of under $t_{ob}\approx\infty$ and $t_{ob}=t_{of}$.

t_{of} (nm)	t_{si} (nm)	λ (μm)		
		For $t_{ob}\approx\infty$	For $t_{ob}\approx t_{of}$	%
5	40	0.0247	0.0175	29.15
5	50	0.0276	0.0195	29.35
5	60	0.0303	0.0214	29.37
10	40	0.0349	0.0247	29.23
10	50	0.0391	0.0276	29.41
10	60	0.0428	0.0303	29.21

The device L_{min} for $t_{ob}=t_{of}$ is about 30% smaller than the $t_{ob}\approx\infty$. Consider a N-channel DGMOSFET as in[1], the threshold-voltage-for-front-gate with surface-region-of-back-gate-depleted $(V_{tf,depb})$ with inverted-back-surface $(V_{tf,invb})$ is expressed as:

$$V_{tf,depb}\left(V_{gb}\right) = Vfbf + \frac{(1+\alpha)(2\Phi_F) - \left(V_{gb} - V_{fbb}\right) + \frac{\beta}{2}\frac{qN_A}{e_{si}}}{\alpha} \quad (3)$$

$$V_{tf,invb} = V_{fbf} + 2\Phi_F + \frac{qN_A t_{si}}{2C_{of}} \quad (4)$$

where V_{fbf} and V_{fbb}: channel-voltages-of-front-back-flat-band, Φ_F: fermi-level-potential, NA: doping-level-for-channel-variations and C_{of}: capacitance-area-of-device-front-gate. Back-gate-threshold-voltage with depleted-surface-at-front-gate ($V_{tb,depf}$ (V_{gf})) and with front-surface-inverted ($V_{tb,invf}$) is similar. For DGMOSFET as $t_{ob}\approx\infty$ and V_{gb}=0. The depleted-surface-at-back-gate and the threshold-voltage-at-front-back-gate is

$$V_{th,soi} = V_{fbf} + 2\Phi_F + \frac{qN_A t_{si}}{2C_{of}} \quad (5)$$

The device V_{th} is 0.38V. V_{gb} =0 and V_{gf} =0 are $V_{tf,0}$ and $V_{tb,0}$ at zero respectively. With a better conductivity of gate surfaces, $V_{tf,0}$ of the device increases by 1/α times V_{gb}. As V_{gb} increases making an an-inverted-region-of-surface-at-back-gate, then the inverted-layer at depleted-surface-at-back-gate becomes a front-back-gates-region-barrier i.e., $V_{tf,invb}$, same analysis for V_{tb} varies with V_{gf}.

For devices with V_{gf} =V_{gb}, V'_{tf} is with threshold, and V_{gb} = V_{tf}. If $V_g < V'_{tf}$, the device is in the subthreshold regime. If $V'_{tf} \leq V_g < V_{tb,invf}$, the front channel will conduct. In this case, V_{tf} changes from $V_{tf,0}$ to $V_{tf,\,dep(Vg)}$. If V_g is larger than $V_{tb,\,invf}$, both channels will contribute to the conduction. V_{tf} will change from $V_{tf,0}$ to $V_{tf,\,invb}$ while V_{tb} from 0 to $V_{td,invf}$. Hence, V_{th} of the device is changed, which benefits the device's condition. When a transistor is "OFF", the threshold voltage is high to suppress the leakage. If it is "ON", the low threshold voltage improves speed.

Another advantage of dynamic thresholds of the device is about supplying voltage scaling. For the device, the minimum supply voltage (V_{min}) can be obtained from $V_{gb} = 2V_{tf}$, which is smaller than $2V_{tf,0}$.

When $V_{min} \leq V_{dd} \leq V_{tb,invf}$, the transistor is an N-channel DGMOSFET, which is a symmetric device with a front channel conducting and a back gate acting as a controlling gate for V_{tf}. If V_{dd} is larger than $V_{tb,invf}$, the device is regarded as a double channel DGMOSFET.

For an N-channel DGMOSFET, the saturation current (I_{on}) as illustrated in Figure 4, is expressed as:

$$Ion = \frac{W\mu_{eff}C_{of}}{2L}\frac{(V_{dd} - V_{tf,vdd})^2}{1 + (V_{dd} - V_{tf}, V_{dd})/\frac{2v_{sat}}{\mu_{eff}}L} \quad (6)$$

$$Ion = \frac{W\mu_{eff}C_{of}}{2L}\frac{(V_{dd} - V_{tf,invb})^2}{1 + (V_{dd} - V_{tf}, V_{invb})/\frac{2v_{sat}}{\mu_{eff}}L} + \frac{W\mu_{eff}C_{of}}{2L}\frac{(V_{dd} - V_{tf,invf})^2}{1 + (V_{dd} - V_{tf}, V_{invf})/\frac{2v_{sat}}{\mu_{eff}}L} \quad (7)$$

The subthreshold current (I_{off}) can be expressed by:

$$I_{off} = I_{f0}\, e^{-\frac{V_{tf,0}}{V_T}}\left(1 - e^{-\frac{V_{dd}}{V_T}}\right) + I_{b0}\, e^{-\frac{V_{tb,0}}{V_T}}\left(1 - e^{-\frac{V_{dd}}{V_T}}\right) \quad (8)$$

Table 2 illustrates I_{on} and I_{off} for a device for different t_{ob}, with V_{dd}=1V, t_{of}=5nm, W/L=1.8/0.25, t_{si}=50nm.

Table 2: I_{on} & I_{off}

Current	Model	t_{ob}		
		30nm	**40nm**	**50nm**
I_{on}	MODEL	3.9e-4A	3.6e-4A	3.4e-4A
	SOISPICE	3.6e-4A	3.4e-4A	3.3e-4A
I_{off}	MODEL	2.1e-10A	1.1e-10A	6.7e-11A
	SOISPICE	1.7e-10A	9.8e-11A	6.9E-11A

In proposed distinct ρ-based DGMOSFET device characteristics as illustrated in Figure 4, power components: dynamic and static are made with the thickness of the device ie, t_{ob} as back-gate-capacitance is reduced with the same DGMOSFET load capacitance.

By reducing t_{ob}, the power components' dissipation reduces and causes the switching speed to increase. And by controlling the leakage power for a symmetric distinct ρ-based DGMOSFET device circuit is used for the low threshold voltage.

For symmetric distinct ρ-based DGMOSFET device circuit, because of the high drive current, the propagation delay is small causing an increase in power dissipation. Distinct ρ-based DGMOSFET device circuits, consumes less power making the symmetric device circuits analyze through propagation delay at a larger rate.

If we consider the power delay product (PDP) between the DGMOSFET device and distinct ρ-based DGMOSFET device, with t_{si}=60nm, t_{of}=10nm, L_{ch} is 0.25μm, A_{switch}=0.3, V_{ss}=1V at 100 MHz frequency, and capacitance between interconnect layers C_{int}=0.2, the distinct ρ-based DGMOSFET device is the best choice.

If PDP = 75% of that of the DGMOSFET device, with interconnect capacitance is high value, the symmetrical distinct ρ-based DGMOSFET device is better. The PDP of symmetric distinct ρ-based DGMOSFET device = 50% of conventional DGMOSFET device.

In summary from the proposed work analysis, the author(s) analyzed and outlines the following observations:

- Distinct ρ-Based DGMOSFET devices have a calibration method with improved grain charge distributions under longer and shorter underlap lengths
- Distinct ρ-Based DGMOSFET devices have better Ion & Ioff characteristics to improve PDP for low power analysis.

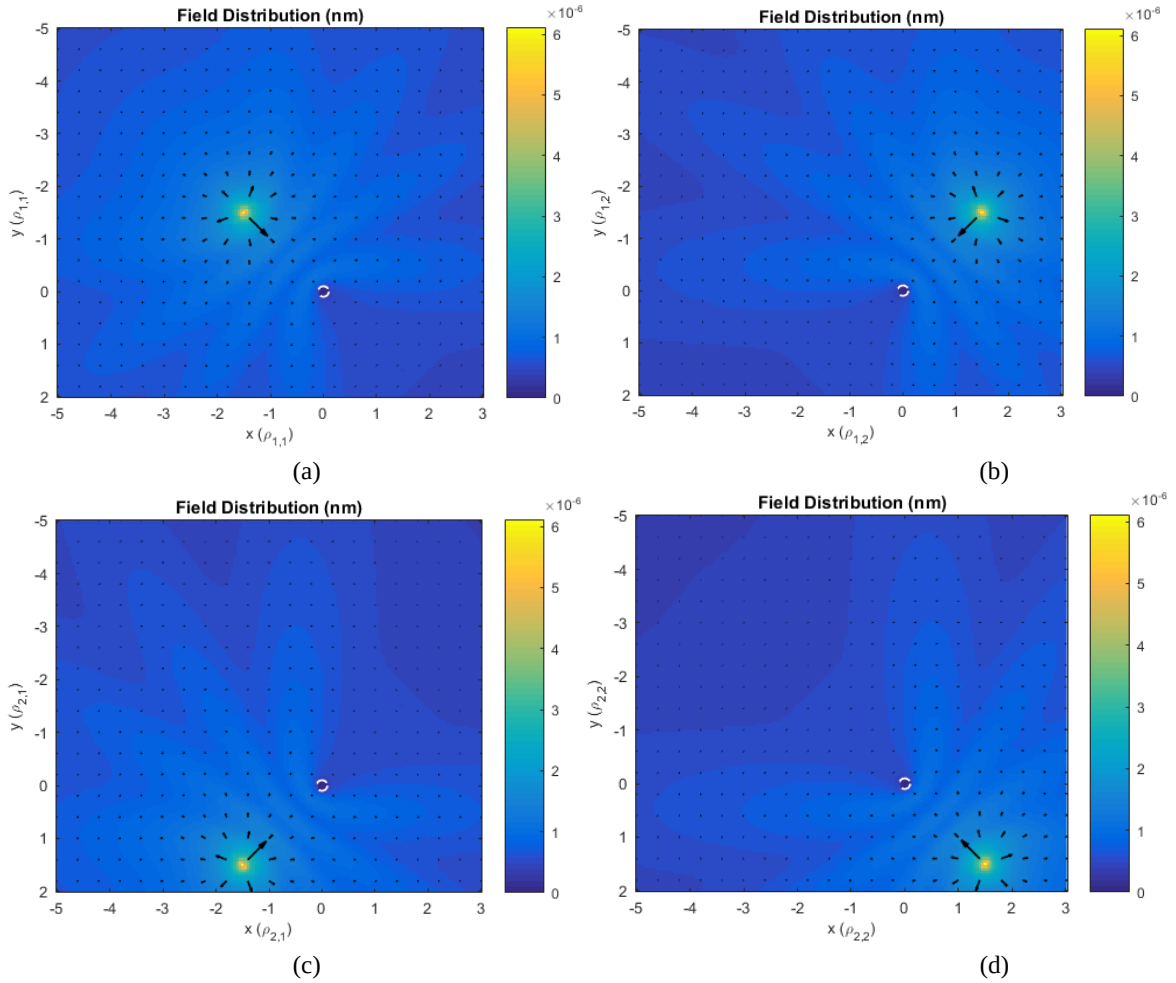


Figure 4. Simulation characteristics of distinct ρ-based DGMOSFET device saturation current (Ion) field distribution under four-grain positions: (a) Illustration of the saturation current (Ion) field distribution for a gate grain position at the left top position, (b) Illustration of the saturation current (Ion) field distribution for a gate grain position at the right top position, (c) Illustration of the saturation current (Ion) field distribution for a gate grain position at the left bottom position and (d) Illustration of the saturation current (Ion) field distribution for a gate grain position at the right bottom position.

DESIGN OF DISTINCT P(RHO)-BASED CAM FOR LOW POWER CIRCUIT DESIGN

A CAM circuit provides the best solution to hardware devices in terms of high-speed search circuits to match and retrieve the circuit device operations. A CAM circuit can perform the direct search by its pre-stored content in a multi-lines way in single-cycle memory access, through in-memory analysis. As shown in Figure 5: designed CAM circuit, the CAM component takes input from a query word and compares it with all the stored patterns in a defined manner or a parallel search pattern and results in a searchable word. In the proposed CAM circuit of SRAM as a memory element holding the pre-stored encoded data with an N-channel DGMOSFETs device, which is a defined selective cell device pre-charge process, which causes low power consumption and area overhead. If any mismatch occurs, then ML discharges to 0, causing all other bits to stay at 1 value even if bits are matched.

To limit this, in this paper, a distinct ρ-element-based CAM implementation is proposed, which utilizes non-volatile logic operands, related to a vector voltage operand and semi-static data operand. These operands are related to resistive element-based designs utilizing a distinct ρ-element operand. In this paper, the operands related to distinct ρ-elements are static voltage CAM cell designs based on gate design and device resistance.

In the proposed distinct ρ-based CAM based Low Power circuit design, shown in Figure 5 and Figure 6, where Figure 5 illustrates AND logic and Figure 6 illustrate OR logic, which focuses on voltage operand and resistance operand, depends on XNOR/XOR gate, is suitable for CAM search index. The design is made for improved performance of mismatch or match operation through memory resistors – memristor devices per voltage operand cell.

During the match condition, as low voltage logic 0 is available as high resistance R_{OFF} at one of the memristors, and at another memristor as high voltage logic 1 is available as low resistance R_{ON}. The combination resistance output voltage is HIGH in this match condition.

During the mismatch condition, as high voltage logic, 1 is available as low resistance R_{ON} at one of the memristors, and at another memristor as low voltage logic 0 is available as high resistance R_{OFF}. The combination resistance output voltage is LOW in this mismatch condition.

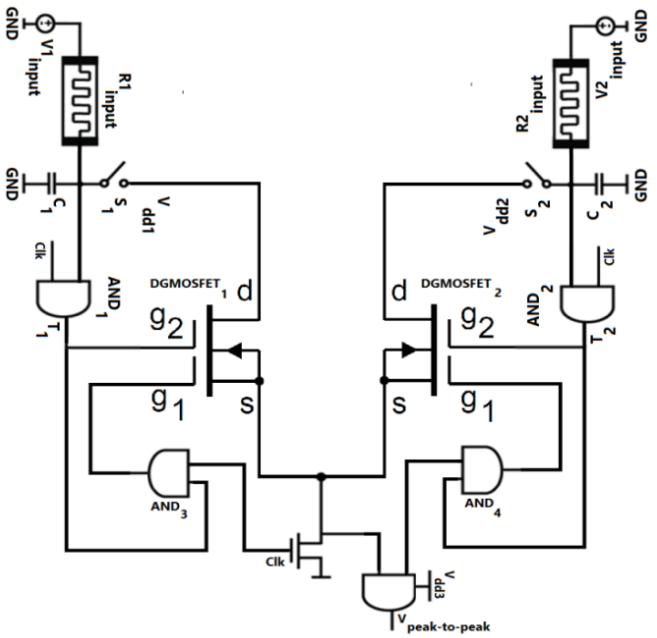


Figure 5. Proposed distinct ρ-based DGMOSFET low power circuit for CAM cell: AND Logic.

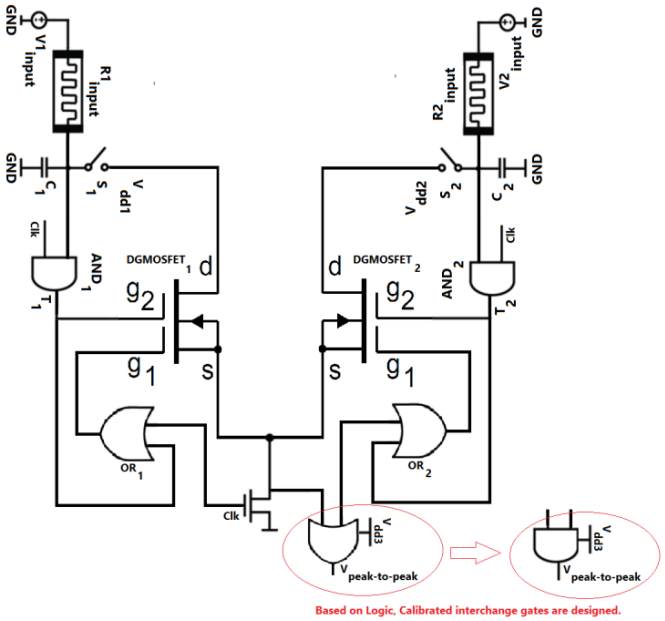


Figure 6. Proposed distinct ρ-based DGMOSFET low power circuit for CAM cell: OR Logic.

In the proposed distinct ρ-based DGMOSFET low power circuit for CAM cell represented with DGMOSFET 1 and DGMOSFET 2, the operation is based on gate terminals 1 and 2 ie., g_1 and g_2, which determine the voltage across each source terminal. The distinct ρ-based DGMOSFET low power circuit for CAM cell contains writing a bit in CAM and searching the bit in CAM operations.

During the write cycle in the CAM cell, if logic 0 is to be stored which makes R_{OFF}=0, a negative voltage is applied at gate terminal g1, which keeps the other gate terminal g_2 based on INV 1 bit value. Then logic 0 is written into the CAM cell of DGMOSFET 1.

During the write cycle in the CAM cell, if logic 1 is to be stored which makes R_{OFF}=1, a negative voltage is applied at gate terminal g_2, which keeps the other gate terminal g1 based on INV 2-bit value. Then logic 1 is written into the CAM cell of DGMOSFET 2.

During the search cycle in the CAM cell, logic 0 is received through AND 1 to the drain terminal d of DGMOSFET 1, at each search cycle. Then INV 1 of DGMOSFET 1 generates two voltage levels as low and high output voltages for each logic 0 input bit from the search word. The low voltage is for the search voltage of the CAM cell for gate g1 terminal to the write bit. The high voltage is for the direction of voltage through DGMOSFET 1 device, which changes depending on the write bit word, and by changing the low and high voltage values, the search cycle can be faster than the conventional CAM.

During the search cycle in the CAM cell, logic 1 is received through AND 2 to the drain terminal d of DGMOSFET 2, at each search cycle. Then INV 2 of DGMOSFET 2 generates two voltage levels as low and high output voltages for each logic 1 input bit from the search word. The low voltage is for the search voltage of the CAM cell for gate g_2 terminal to the write bit. The high voltage is for the direction of voltage through DGMOSFET 2 device, which changes depending on the write bit word and by changing the low and high voltage values.

These low and high voltages through INV 1 and INV 2 are the voltage operands to the proposed distinct ρ-based DGMOSFET low power circuit for the CAM cell, which stores the logic voltage levels based on the resistance operand. The output V peak-to-peak from each INV 1 and INV 2 reflect the write cycle and search cycle operation, for INV 1 output voltage in the DGMOSFET 1 device generates a time-domain voltage pulse signal using DGMOSFET 1 device section. And the produced time-domain voltage pulse signal is combined through the voltage-domain time pulse signal and passed through INV 2 for output voltage in the DGMOSFET 2 device, to determine the two operands with voltage pulse to generate time base V peak-to-peak signal.

A. Analysis of Read and Write Operations Improvement in Distinct ρ (Rho)-Based TCAM Circuit

Binary CAM cells a logic 0 or a logic 1 value, while ternary CAMs store an additional X value, which is a-don't-care-condition, representing 0 & 1, for a third state condition, which stores a-match-word based on input-bit-condition, by representing D and D' as two bits in complementary notations. These two bits represent four possible state values, but in the case of TCAM, we make use of these three-states, where the state of D=D'=0 is not considered in the analysis. For TCAM value storage, a second SRAM cell and NOR cell are used. The bit D is at the left-pulldown-path and bit D' is at the right-pulldown-path, by this both-paths of bits D and D' are independently controlled.

During the condition D=D'=1, the value result condition X will be stored in the CAM cell, which makes both D and D' pulldown paths disable and makes the cell have a logic 1 value regardless of D and D' input state values.

During the condition D=1 and D'=0, the value result condition 1 will be stored in the CAM cell, which makes either D or D' have pulldown paths to enable and makes the cell have a logic 1 value for D and D' input state values.

During the condition D=0 and D'=1, the value result condition 0 will be stored in the CAM cell, which makes either D' or D have pulldown paths to enable and makes the cell have a logic 0 value for D and D' input state values.

During conditions D=0 and D'=0, the value result condition is not considered in this analysis.

When we store X value, the search line will search for the stored X value by making SL logic and SL' logic as 0, that the condition is with an external-don't-care condition which forces a bit-match for the stored bit. The possibility of storing X is made in TCAM by the use of condition D=D'=1, where only ternary CAM operation is possible, not binary CAM operation. To perform for binary, we require performing the ternary operation on two binary cells for each ternary CAM cell used.

In the proposed work, the ternary CAM cell is implemented using the pulldown transistors M1-M4 using pMOS devices and use search-lines and match-lines in complementing values of its logic levels.

B. Low Power Analysis

Using N-channel DGMOSFETs transistors instead of traditional DGMOSFETs, as proposed in this paper, for the comparison analysis the device circuit allows a compact design for circuit layout, with the reduce in amount-of-spacing among p-and-n-diffusions in the device. As the density increases, a small amount of area reduces further at wiring capacitances & which reduces the power consumption.

In the proposed work, this power reduction tradeoff results from the use of minimum-size N-channel DGMOSFETs transistor instead of the minimum-size transistor, by this the pulldown path have a lower pulldown resistance and increases the search operation.

The operation of the NAND cell is designed through a mask element for bit storage at node M. During ternary operation, for X value to store, mask element for bit storage = 1. Making the device M_{mask}=ON, through the value of D, making the device match the line. During X value storage in the CAM cell, the searching line CAM makes X through SL and SL' = 1.

The NAND match-line process is a process of SL and ML with less power utilization of the previous device logic state. At the matching transistor of the nMOS chain, only one device match line is in match state, which is having only one transistor in the matching device chain of match lines that is ON and thus only a small amount of power is utilized by the device. Thus the match line power dissipation is reduced, which makes advantages in reducing power-consumption for device CAM model design.

In the proposed work, a power-saving method through selective cell device pre-charge is implemented. Here, at the first stage, the match operation of the first few bits of a word is made with the remaining bits. In the second stage, the match operation bits are used for the remaining bits to operate, which reduces mostly 89% of the match line power operation. In the third stage, the overheads in the matching speed are limited by drawing a good amount of power in the first stage and reducing the power consumption in the second stage, causing the speed of operation to increase. And in the fourth stage, the distributed bits in CAM cells are made with initial match bits by making identical stored bit values in CAM, which eliminated the further power usage for search lines and match lines.

From the above proposed CAM cell analysis, the author(s) have observed the design of distinct ρ-Based DGMOSFET CAM cells to enhance the conventional CAM cell designs discussed.

To summarize the proposed work analysis, the author(s) analyzed and outlines the following observations:

- Distinct ρ-Based DGMOSFET CAM cells can increase the mismatch lines up to 256 bits with a data pattern length of more than 73% of accuracy.
- Distinct ρ-Based DGMOSFET CAM cell generates a pattern of data query to have high match line(s) and accurate mismatch line(s).

Simulation Results and Discussion Of Proposed Model

This section explains the simulation analysis of the proposed distinct ρ-based CAM-based Low Power circuit design structure. Through TCAD simulations, the variations of Quantum Confinement (QC) effects on channel parameters such as the sub-threshold slope of proposed DGMOSFET with a varying channel length (L_{ch}) from 10nm to 30nm. The structure of the distinct ρ-based DGMOSFET device calibration model is shown in Fig 1., where it can be observed that the variation of scalable channel length to 30nm can be varied by making the SOI channel and oxide thickness thin, causing the thickness of channel silicon to reduce and increase in quantum confinement effect, where channel electrostatics were impacted. These observations were shown in table 3, where an electrostatics parameter I_{on} / I_{off} Ratio is illustrated as a function of the channel variation for linear subthreshold swing and saturation subthreshold swing for analysis of QC effects for different values of t_{oxf} and t_{oxb}.

From the simulation of the proposed distinct ρ-based DGMOSFET device, the results shown in table 4, clearly demonstrate that with an increase in L_{ch} with the varying channel thickness t_{ch} and t_{ox}, the formation of conduction layer between gates to channel increases, results in a decrease in the sub-threshold slope values. By varying the channel parameters t_{ch} and t_{ox} at higher values from 15nm to 25nm, the electric field distribution of transverse electric along the gate increase when we compare with the simulation along the lateral electric distribution of the electric field from the drain.

From these two lateral and transverse electric field distributions, coupling between the channel and gate increases and decreases in sub-threshold slope values. With the further decrease in QC effects, the transverse electric field distribution still increases causing the longitudinal electric field distribution to decrease nominally from the drain channel region, which decreases further sub-threshold slope compared to the high value of QC effects, as shown in table 4, for different values of t_{ch} and t_{ox}. Therefore, for a given QC affects variations the channel electrostatics are effected with nominal change, causing the effects to be considered in the design of the proposed distinct ρ-based DGMOSFET device.

It is clear from the analysis of table 4, that while the greater scalability of the proposed distinct ρ-based DGMOSFET device is made possible through the increased values of t_{ch} and t_{ox}, results in the reduced effects of QC on channel length electrostatics characteristics with a limit on device scalable channel lengths.

A. Channel Length

For better analysis, the work function of front gate 1 to the back gate is 4.5 eV and the work function of front gate 2 to the back gate is 4.9 eV.

In table 3, the channel length parameter of the ON state of R_{ds} is analyzed, which is the crucial current rating parameter of a distinct ρ-based DGMOSFET device. Mostly for the lesser value of $R_{ds(ON)}$, between the source and drain the current losses are reduced causing the $R_{ds(ON)}$ to reduce, in-turn the power dissipation is reduced through the current-passing-through the device channel. If the same L_{ch} is increased, making $R_{ds(ON)}$ increases, reducing the current drawing efficiency.

So, varying the L_{ch} for the device can reduce the SCEs, and the current of $R_{ds(ON)}$ can be increased. In the simulation, the channel lengths are varying-from-10 nm-to-30 nm, and identified that L_{ch} with 10nm (smaller), the smaller the $R_{ds(ON)}$ resistance, which improves the drive current with lesser threshold voltage requirements and provides more change carriers at pinch off regions.

To obtain the improved drive current from the designed proposed distinct ρ-based DGMOSFET device as shown in table 3, channel length values are set to 20nm, with a work function of Gate1 and Gate2 as 4.2ev and the doping concentration of channel, drain and the source is 10^{19} cm^{-3}. And to have a reduced thickness of dielectric material, we consider the gate oxide thickness to a minimum of 2nm to reduce short channel effects and leakage current in the gate.

In the proposed distinct ρ-based DGMOSFET device, the high-k dielectric material is used to increase the gate capacitance, causing the gate channel to reduce the leakage current and reduce the SCEs. For varying channel length(s), the value of $R_{ds(ON)}$ affects the current losses between the source and drain. The low value of $R_{ds(ON)}$, reduces the current losses between the source and drain causing the current passing through the channel to reduce, making the device work at low temperatures.

For a channel length of more than 15nm, the high value of $R_{ds(ON)}$ increases the current losses between source and drain causing the current passing through the channel to increase, which mitigate short channel effects causing the ON current to increase gradually.

For a channel length less than 15nm, the $R_{ds(ON)}$ gives an improved drive current and by this short channel makes lesser threshold voltages to supply more charge carriers to pinch-off regions.

Table 3: Performance values of the proposed distinct ρ-based DGMOSFET structure for CAM design.

Channel Length(nm)	I_{off} (A/µm)	I_{on} (A/µm)	I_{on}/I_{off} Ratio
10	$10^{-12.42}$	5.89 x 10-4	5.89 x 10^{-8}
15	$10^{-12.26}$	5.72 x 10-4	5.72 x 10^{-8}
20	$10^{-12.01}$	4.55 x 10-4	4.55 x 10^{-8}
25	$10^{-11.89}$	4.12 x 10-4	4.12 x 10^{-7}
30	$10^{-11.76}$	3.74 x 10-4	3.74 x 10^{-6}

B. Device Characteristics Comparisons

Table 4 illustrates the comparison of key parameters of the proposed distinct ρ-based DGMOSFET device with INVERTED-T and Si-Ge FET devices. Compare to other devices with a reduced LG value, the proposed distinct ρ-based DGMOSFET device shows a better low I_{on}/I_{off} Ratio value compared to the Si-Ge device. Also an improved subthreshold swing (SS_{linear}(mV/dec) and subthreshold swing (SS_{linear}(mV/dec) values compare to the Inverted-T device.

Figure 1 shows the physical structure of a distinct ρ-based DGMOSFET device calibration model. At the first, the mono-crystal-Si-layer of a p-type-SOI-wafer is layered to 15 nm, and a 10-nm-thick epitaxial SiGe layer and 40-nm-wide channel masks are grown.

Next, a 4-nm-thick gate dielectric oxide layer is deposited, subsequently, the source and drain regions are implanted at a dosage of 1 x 10^{12} cm^{-2} and energy of 10keV. In the final step, dopant activation and gate oxide crystalline are made. Fig 4 shows the characteristics of distinct ρ-based DGMOSFET device saturation current (I_{on}) field distribution under four-grain positions for the transfer drain current I_D - gate voltages V_G analysis, including both forward and reverse characteristics including gate length (L_G) and channel width (W_{ch}) at drain voltage V_D= -0.05 V; with normalized I_D value.

The proposed distinct ρ-based DGMOSFET device calibration model exhibits a steep subthreshold swing (SS) in the range of drain currents. The average value of SS calculated by one decade of I_D increasing has a minimum of 61.9mV/ dec. The I_{on} / I_{off} ratio value shows near the measure limitation with different values of t_{oxf} and t_{oxb}.

Table 4, represents the SS_{linear} and $SS_{saturation}$ with I_{on} / I_{off} Ratio, where SS was considered from every value of I_{on} / I_{off} Ratio. The proposed device exhibits a SS value of less than 62mV/dec. The proposed distinct ρ-based DGMOSFET device exhibited SS_{avg} of 62.35 mV/dec, V_T of -0.27 V, drain-induced barrier lowering (DIBL) of 2.2 mV/V, on current I_{on} (A/µm) of 4.55 x 10-4, and on-off current ratio (I_{on}/I_{off} Ratio) of 4.55 x 10-8, I_{on} and I_{off} is extracted at V_D=-1V and V_G=0V.

These results show that the distinct ρ-based DGMOSFET device channel can reduce SCE with adequate current values. Table 4, shows the TCAD simulation of SiGe DGMOSFET, where the V_D= -0.1 V and V_G=-1V have a hole current density based on SiGe conductivity at the front gate with higher current density and on Si conductivity at the back gate with lower current density.

After the formation of the channel between the front and back gate, the current densities of the channel two layers were found to be having equal amount to total current with a lower thickness of SiGe conductivity of the front gate compared to a higher thickness of SiGe conductivity of the back gate, causing hole carriers to drift between the front gate and back gate, having the overall characteristics a steep SS_{avg} of 62.35 mV/dec.

Table 4: Characteristics Comparative results of DIBL in proposed distinct ρ-based DGMOSFET with INVERTED-T [36] and Si-Ge [46] FET devices

Parameter	INVERTED-T	Si-Ge	Proposed distinct ρ-based DGMOSFET
Channel Structure	Inverted-T	Nono-sheet	Distinct- ρ
Channel dimension (upper (nm) x lower(nm))	16 x 14 and 40 x 18	100 x 5	16 x 12
Gate Length (L_G) (nm)	60	55	40
I_{on}/I_{off} Ratio	1.7x10^7 @ V_D=-1V	~9x10^6 @ V_D=-0.5V	2.54 x 10^{-6} @ V_D=-0.6V
Subthreshold swing (SS_{linear}(mV/dec)	59.1	65	62.8
Subthreshold swing ($SS_{saturation}$(mV/dec)	60	67	61.9

Further, a reduction in the value of I_{on}/I_{off} Ratio can be done by reducing the L_G value, which makes the proposed distinct ρ-based DGMOSFET device a better device for low-power applications.

C. CAM Match Comparisons

Table 5 provides the comparison of energy consumption/bit of the proposed distinct ρ-based CAM with conventional CAM and HD-CAM. For comparative analysis, supply voltage and word size are taken as 1.2 V and 256 bits for all three methods. In comparison with conventional CAM, the proposed distinct ρ-based CAM has

shown less energy consumption at bits=16 and the same amount of consumption at bits=128.

In comparison with HD-CAM, the proposed distinct ρ-based CAM has shown less energy consumption at bits=16 and the same amount of consumption at bits=64. This better performance of the proposed distinct ρ-based CAM is attained by performing an estimated search operation, with the reduced match-line discharge time.

To provide an improved match and mismatch for a configured CAM cell as shown in Figure 5, and Figure 6, with some mismatching bits, which can be overcome in the proposed distinct ρ-based DGMOSFET low power circuit for CAM cell.

Here the mismatch criteria are considered between two definite integer values as p and q, where p is the number of mismatching bits in the proposed distinct ρ-based DGMOSFET low power circuit for CAM cell and q is the number of matching bits in distinct ρ-based DGMOSFET low power circuit for CAM cell. The value of p is defined as ≤p, with a range of certain regions; the presence of true mismatch may occur. The value of q is defined as ≥q, with a range of certain regions; the presence of a true match may occur. The values of a region between p and q are defined as ≥q:≤p, with the range of uncertain region; the presence of a false match or a false mismatch may occur. Fig 5 and 6 show the schematic of the proposed distinct ρ-based DGMOSFET low power circuit for CAM cell: OR Logic & AND Logic respectively, which can perform search operations. The CAM cell used is based on the NAND-type CAM bit cell, with the presence of ρ-elements (ρ_{R1C1}) used to control the ML discharge rate, based on the value of the ρ-voltage (V_{R1C1}). When the ρ-elements are driven with maximum driving voltage ie., V_{R1C1}=VDD, an exact match is possible at the p condition. When the ρ-elements are driven with a minimum driving voltage ie., V_{R1C1}<VDD, an appropriate match is possible at q condition. When the ρ-elements are driven with an approximate driving voltage ie., V_{R1C1}<=V_{DD}, an exact match or exact mismatch is possible at p and q conditions. For these cases, the operating principle is: the SL and SL' are driven to a low value, then ML is pre-charged to V_{DD}, and the search pattern is made available to SLs for ML. If the ML value is above ρ_{R1C1} level, then a match is possible; otherwise, a mismatch is possible. For data-bit analysis, pre-load D='1' for an 8-bit ρ-elements-CAM word, for a search operation, a single-bit mismatch occurs for D and SL values to complete the discharge of ML, making ML a high value. Likewise, for every approximate search, the value of ML increases with every single mismatch bit. This approximate match search depends on ρ_{R1} conductivity levels, which play a major role in match operation. When V_{R1C1} value is low, the mismatch cells could discharge C_1 in ρ_{R1C1} conductivity levels during the matching time. This makes a shorter matching time to do exact match operations. When V_{R1C1} value is lower than V_{DD}, the mismatch cells could discharge C_1 with R_1 in ρ_{R1C1} conductivity levels during the matching and mismatching time. This makes a shorter matching time and approximate mismatching time to do exact match operation. For longer words-data patterns, a larger V_{R1C1} value is considered which impacts the mismatch cells to discharge C_1 in several bit-cells, this makes an approximate matching time to do an exact match operation. From the above results analysis discussion, the proposed distinct ρ-based DGMOSFET low power circuit for CAM cell design reduces the delay overhead compared to conventional NAND and NOR schemes and provides very less mismatch levels, and maintains better efficiency across V_{R1C1} values.

Table 5: Comparative results of energy consumption/bit in proposed distinct ρ-based CAM with conventional CAM [47] and HD-CAM [29]

Parameters	**CAM (For V_{DD}=1.2V)**	**HD-CAM (For V_{eval}=0.6V)**	**Proposed distinct ρ-based CAM(For V_ρ =0.6V)**
	Energy consumption/bit		
Supply voltage, V_{DD} (V)	1.2	1.2	1.2
Word size	256-bit	256-bit	256-bit
Bits=16	0.509	0.507	0.495
Bits=64	0.619	0.618	0.618
Bits=128	0.766	0.765	0.766
Evaluation time (ns)	1	1	1

From the above proposed CAM cell analysis, the author(s) have observed the design of the proposed CAM cell model to reduce the energy consumption and sub-threshold swing compare to the conventional designs discussed.

To summarize the proposed work analysis, the author(s) analyzed and outlined the following observations:

- Distinct ρ-Based DGMOSFET CAM cell model with smaller L_{ch} (10nm), the lower the $R_{ds(ON)}$ resistance, which improves the drive current with lesser threshold voltage requirements and low power dissipation.
- Distinct ρ-Based DGMOSFET CAM cell models have a better low I_{on}/I_{off} Ratio value with an improved subthreshold swing (SS_{linear}(mV/dec) and subthreshold swing ($SS_{saturation}$(mV/dec) values.
- Distinct ρ-Based DGMOSFET CAM cell models have shown less energy consumption at bits 16, 64, and 128 by performing an estimated search operation, with the reduced match-line discharge time.

CONCLUSIONS

In this paper, a distinct ρ-based DGMOSFET low-power circuit for CAM cells with operands related to distinct ρ-elements for efficient low-power computation is proposed. The proposed design has three main design steps: to design a distinct ρ-based DGMOSFET device for the calibration model, to design a low-power distinct ρ-based DGMOSFET device, and to design a CAM circuit design using the low-power distinct ρ-based DGMOSFET device. The low-power CAM cell takes logic operands, related to a vector voltage operand and semi-static data operand. These operands result in an output voltage $V_{peak\text{-}to\text{-}peak}$ which is a pulse width through logic operands.

The proposed distinct ρ-based DGMOSFET low-power circuit approach for CAM cells with operands provides better device area utilization and energy savings compared to conventional CAM.

FUTURE SCOPE

In this paper, a distinct ρ-based DGMOSFET low-power circuit for CAM cells with operands is proposed through a calibration model for an improved DG MOSFET model through SCEs parameters I_{on}/I_{off} ratio and linear subthreshold swing, which makes the device focus on future implementation to the fabrication process of distinct ρ-based DGMOSFET low power circuit for CAM cell.

The future applicability potential of the proposed method is illustrated below:

- Illustrated work in this research work is applied to fully depleted DG MOSFET in developing and improving channel electrostatics with scalable thinner channels and oxide thicknesses.
- Implementation of proposed work in emerging transistor Sub-nm technologies, specifically DGMOSFET, can realize compact and energy-efficient ternary content addressable memories (CAM).
- These requirements of Sub-nm VLSI technology are implicated in leakage current and power analysis for memory design, which suffers from timing violations, our proposal will be evaluated in the future.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Hameed Pasha Mohammad (HPM) and H. C. Hadimani (HCH) identified, conducted, and analyzed the research; HPM and HCH wrote the paper; Udara Yedukondalu and Srinivasa Rao Udara reviewed the paper; all authors had approved the final version.

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